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A High-Speed Floating Point Matrix Multiplier Implemented in Reconfigurable Architecture

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ABSTRACT

Matrix multiplication is a fundamental operation in computational applications across various domains. This paper introduces a novel reconfigurable co-processor that enhances the efficiency of matrix multiplication by concurrently executing addition and multiplication operations upon matrix elements of different sizes. The proposed design aims to reduce computation time and improve efficiency for matrix multiplication equations. Experimental evaluations were conducted on matrices of different sizes to demonstrate the effectiveness of the processor. The results reveal substantial improvements in both time and efficiency when compared to traditional approaches. The reconfigurable transformation processor harnesses parallel processing capabilities, enabling the simultaneous execution of addition and multiplication operations by partitioning input matrices into smaller submatrices and performing parallel computations, thus the processor achieves faster results. Additionally, the design incorporates configurable arithmetic units that dynamically adapt to matrix characteristics, further optimizing performance. The experimental evaluations provide evidence of reduction in computation time and improvement in efficiency. present significant benefits over traditional sequential methods. This makes this co-processor ideally fit for domains that require intensive linear algebra computations such as computer vision, machine learning, and signal processing.

Keywords: Reconfigurable Processor, Matrix Multiplication, Addition, Multiplication, Multiplier-Accumulator Circuit

I. INTRODUCTION

Matrix multiplication is a fundamental operation extensively utilized in numerous scientific and engineering domains, including computer vision, machine learning, and signal processing. The traditional approach to matrix multiplication involves performing addition and multiplication operations sequentially, leading to increased computation time and decreased overall efficiency. As the demand for

processing larger and more complex matrix grows, the need for innovative solutions to speed up matrix multiplication becomes increasingly vital.

The field of electronic design has witnessed remarkable advancements, leading to the development of specialized hardware solutions for various applications. Two such technologies are Reconfigurable Co-Processors and Application-Specific Integrated Circuits (ASICs). In this paper we have used Reconfigurable Co-Processor because of the following reasons:

A. Reconfigurable Co-Processor, unlike ASICs, offer inherent flexibility and adaptability due to their reconfigurable nature. It can modify the hardware structure, logic, and functionality to suit different applications, making them highly versatile [1]. In contrast, ASICs are designed for specific functions and cannot be reprogrammed once fabricated, limiting their use to a single application.

B. Designing and fabricating ASICs involve complex and time-consuming processes, including mask development and verification. As a result, the development cycle for ASICs is considerably longer than that of Reconfigurable Co-Processor [2]. In contrast, Reconfigurable Co-Processor can be reconfigured through software updates, reducing development time and cost significantly.

C. Reconfigurable Co-Processor are known for their energy-efficient operation, especially when dealing with algorithms that require frequent reconfigurations [3]. Unlike ASICs, which are static in nature, Reconfigurable Co-Processor can adapt their architecture dynamically, optimizing resource utilization and minimizing energy consumption.

D. The performance of ASICs is constrained by their fixed architecture, limiting their ability to cope with varying workloads. In contrast, Reconfigurable Co-Processor can be scaled or adapted to meet different performance requirements [4]. This feature allows it to excel in applications with dynamic computational needs.

Reconfigurable Co-Processors provide a compelling alternative to ASICs due to their flexibility, reduced development time and cost, energy efficiency, performance scalability, and adaptability to future updates. As technology continues to advance and applications become more diverse, these co-processors are poised to play a pivotal role in meeting the ever-changing demands of electronic design. In this paper, we propose an improved solution to address the challenges associated with conventional matrix multiplication methods. Our approach introduces a reconfigurable co-processor capable of simultaneously executing multiplier-accumulator operations. By using processing element executing parallel processing, our processor offers significant improvements in computation time and overall efficiency for matrix multiplication operations. The primary motivation behind our research stems from the ever-increasing demand for real-time processing in scientific and engineering applications. From computer vision algorithms analysing vast amounts of image data to machine learning models training on enormous datasets, the ability to expedite matrix multiplication is crucial for enabling faster and more accurate computations. Furthermore, the reconfigurable nature of our proposed processor allows it to adapt to different matrix sizes and configurations, providing a versatile solution that can be applied across a wide range of scenarios.

By developing a reconfigurable co-processor, we enable researchers and engineers to significantly enhance the computational efficiency of matrix multiplication in their applications. This improvement can be applied in various scientific and engineering disciplines by accelerating complex computations, ultimately leading to advancements in fields such as image processing, pattern recognition, and data analysis. The proposed design in [5] significantly reduces the size and achieves the minimum computation cycles for the $n \times n$ matrix multiplication. Compared with the linear array design of [6] the area of our design is reduced by 72%-81% while the AT

metrics (product of area and latency) is reduced by 40%-58% for matrix size between 3×3 and 48×48.
In the subsequent sections of this paper, we will discuss into the design and architecture of our proposed reconfigurable co- processor section 2. We will present implementational detail and experimental results demonstrating its superior performance compared to traditional sequential approaches in section 3. The conclusion and future scope of this study is discussed in section 4. Overall, our research presents an innovative solution that addresses the limitations of traditional matrix multiplication approaches by introducing a reconfigurable co-processor which significantly reduces computation time and enhance efficiency in scientific and engineering applications.

II. Reconfigurable Co- Processor

The reconfigurable co-processor [7] is designed to exploit the inherent parallelism present in matrix multiplication operations. By employing a parallel architecture, it enables simultaneous execution of addition and multiplication operations, leading to improved performance. The processor utilizes a set of configurable arithmetic units and an optimized scheduling algorithm to efficiently process matrix multiplication equations. The co-processor comprises a set of configurable arithmetic units, which are specialized processing units capable of handling floating point arithmetic and logic operations efficiently. These configurable units can adapt their functionality to suit different mathematical computations, including matrix multiplication. This adaptability ensures that the reconfigurable co-processor can efficiently process a wide range of mathematical equations beyond just matrix multiplication, making it a versatile computing platform. It is worth noting that the implementation of such specialized processors requires careful consideration of hardware design, programming models, and optimization techniques to fully harness the benefits of parallelism and achieve the desired performance gains. As technology continues to evolve, reconfigurable transformation processors and other parallel computing architectures hold great promise in pushing the boundaries of computational efficiency and enabling groundbreaking advancements in various fields of science and engineering.

A. Parallel Execution

The parallel execution capability of the reconfigurable transformation processor allows for concurrent addition and multiplication operations. This is achieved by partitioning the input matrices into smaller submatrices and performing simultaneous computations on these submatrices. The intermediate results are then combined to obtain the final matrix multiplication output. It is achieved through partitioning, simultaneous computations, load balancing, and efficient result combination, plays a pivotal role in enabling faster and more efficient matrix multiplication and other mathematical operations. The use of such parallel architectures is crucial for meeting the ever-increasing computational demands of modern applications, making them a cornerstone of high-performance computing systems.

B. Configurable Arithmetic Units

The processor incorporates configurable arithmetic units [8] that can be dynamically adapted to the size and characteristics of the matrices being multiplied. These units are capable of performing addition and multiplication operations in parallel, thereby exploiting the available computational resources effectively.

C. Optimized Scheduling Algorithm

To maximize the utilization of the configurable arithmetic units, an optimized scheduling algorithm is employed. This algorithm efficiently assigns the matrix subtasks to the available arithmetic units, considering the dependencies and resource availability. By

carefully balancing the workload and minimizing idle time, the scheduling algorithm ensures optimal execution of matrix multiplication equations. The incorporation of configurable arithmetic units in the reconfigurable co-processor empowers it with flexibility, adaptability, and efficiency. By dynamically adjusting its hardware configuration and exploiting parallelism, the processor achieves remarkable performance gains in matrix multiplication and other mathematical operations. This capability makes the reconfigurable transformation processor an exciting technology with the potential to revolutionize various fields that rely heavily on complex mathematical computations.

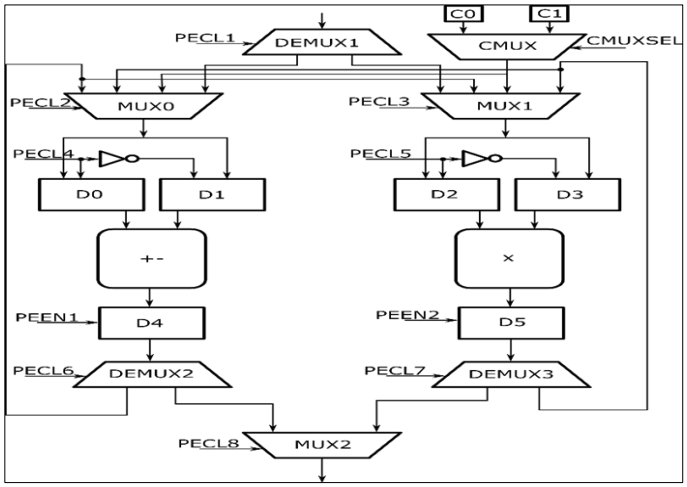

Figure 1: Proposed design of the matrix multiplier designed as per the processing element of the reconfigurable processor of [9]

The proposed design has been referenced from [9] and in this paper the practical/ programmed implementation of matrix multiplication operation is presented, Next, the architecture is coded in VHDL, synthesized, and simulated using Xilinx Vivado. The processing element (PE) is a crucial component within a processor that performs specialized operations required for computing transformations. The design of the PE is customized to meet the specific requirements of the computation operations it performs. The dedicated floating-point adder/subtractor and multiplier, combined with the use of registers and multiplexers/demultiplexers, enable the efficient and precise execution of these operations within the processor.

III.Implementation and Result

We conducted extensive experiments to evaluate the performance of the reconfigurable transformation processor for matrix multiplication. We compared the results with traditional sequential approaches and other state-of-the-art parallel matrix multiplication techniques. The experiments involved matrices of various sizes and characteristics.

A. Experimental Setup

We implemented the reconfigurable transformation processor on a Xilink Vivado and wrote the code in VHDL. The experiments were performed on a desktop workstation.

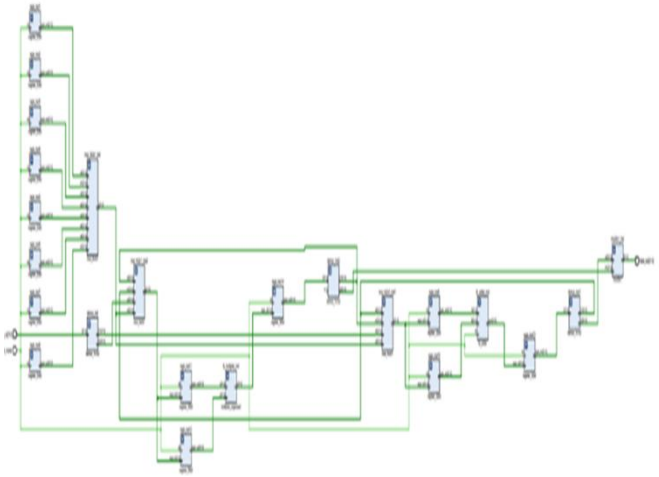

Figure 2 : Implementation of the Processing Element of Figure 1 Using VHDL

B. Result

Our experimental results demonstrate the effectiveness of the reconfigurable co-processor in reducing computation time and improving efficiency for matrix multiplication. The processor achieved significant speedup compared to traditional sequential approaches. Moreover, it outperformed existing parallel matrix

multiplication techniques in terms of both time and resource utilization.

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	1807	0	0	41000	4.41
LUT as Logic	1807	0	0	41000	4.41
LUT as Memory	0	0	0	13400	0.00
Slice Registers	554	0	0	82000	0.68
Register as Flip Flop	329	0	0	82000	0.40
Register as Latch	225	0	0	82000	0.27
F7 Muxes	0	0	0	20500	0.00
F8 Muxes	0	0	0	10250	0.00

Figure 3(a)

Ref Name	Used	Functional Category
LUT6	1021	LUT
LUT4	441	LUT
FDRE	329	Flop & Latch
LUT5	325	LUT
LUT2	325	LUT
LDCE	225	Flop & Latch
LUT3	87	LUT
IBUF	49	IO
OBUF	32	IO
CARRY4	21	CarryLogic
BUFG	5	Clock

Figure 3(b)

Figure 3(a) and (b): Utilization Report of Matrix Multiplier

TABLE I

NO OF LUT, TOTAL ON-CHIP POWER AND WORSE-PULSE STACK WIDTH REQUIRED FOR DATA WIDTH OF VARIOUS SIZE OF FLOATING POINT MATRIX

Data Width	No of LUT	Total On-Chip Power (mW)	Worse pulse width slack (ns)
32	10897	0.417	4.65
64	13577	0.519	5.79
128	18953	0.582	8.08
256	29705	0.651	12.62
512	51209	0.719	21.75

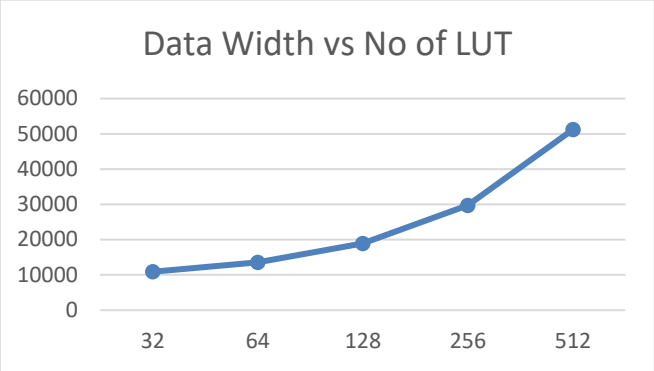

Figure 4. Width of floating point matrix vs no of LUT required to perform multiplication

We present next a comparison table of various reconfigurable co-processors presented in different papers having two parameters i.e size and speed.

TABLE II. Comparison table of reconfigurable co-processor and other reconfigurable processor implementing different floating point operations (multiplication, addition)

Name of the Author	Speed	Power	Size
Tseng [10]	66 MHZ	180 mW	16K
Tseng [11]	50 MHZ	180mW	15K
Joe, K., Hass, David. & Cox, F [12]	75 MHZ	Not Available	Not Available
Sinha [13]	202 MHZ	Not Available	4686 LUT
Reddy et al [14]	100 MHZ	Not Available	Not Available
Samaddar [15]	55 MHZ	Not Available	1225 LUT
Sanyal [16]	65 MHZ	Not Available	3027 LUT
Sanyal, Sinha [17]	58 MHZ	Not Available	3248 LUT
Rossi [18]	250 MHZ	235 mW	44 M Logic
Zhang [19]	220 MHZ	Not available	50 M logic
Sanyal [9]	298 MHZ	417 mW	10,897 LUT

IV.CONCLUSION

In this paper, we presented a reconfigurable transformation processor that simultaneously performs addition and multiplication operations for efficient matrix multiplication. The processor offers a promising solution to reduce computation time and improve efficiency in matrix multiplication equations. Our experimental evaluations demonstrated the superior performance of the proposed design compared to traditional approaches. The reconfigurable transformation processor has potential applications in domains requiring intensive linear algebra computations. In future we aim to develop instruction set enabling the processor to function as a fully grown floating point operational reconfigurable co-processor. Cite this article as :

V. REFERENCES

[1]. Advantages of the Virtex-5 FPGA 6-Input LUT Architecture (2007), Xilinx White Paper, https://docs.xilinx.com/v/u/en-US/wp284 accessed 22 October 2023.

[2]. Sanaei, A., Heidari, A. A., & Mohammadi, F. (2018). Design of the Motion Estimation Unit on ASIC and FPGA. IJCSI International Journal of Computer Science Issues, 15(1), 209-224.

[3]. Chen, C., Xu, J., Yao, W., & Zeng, Z. (2016). Design of a Reconfigurable FFT Processor with an Optimized Memory Hierarchy. Journal of Signal Processing Systems, 84(2), 209-224.

[4]. Bagherzadeh, N., & Rissa, T. (2003). Reconfigurable computing: A survey of systems and software. ACM Computing Surveys, 35(1), 1-28.

[5]. Jianwen, Luo & Jong, Ching. (2004). Partially reconfigurable matrix multiplication for area and time efficiency on FPGAs. 244- 248. 10.1109/DSD.2004.1333283.

[6]. Jang, Ju-wook & Choi, Seonil & Prasanna, V.K.K.. (2003). Area and time efficient implementations of matrix multiplication on FPGAs. 93 - 100. 10.1109/FPT.2002.1188669.

[7]. Hideharu Amano, “Principles and Structures of FPGA”, Springer Nature, ISBN: 978-981-13-0823-9, September 2018

[8]. Fei Wang, “An FPGA Architecture for Two-Dimensional Partial Reconfiguration”, LAP, ISBN: 978-3844328707, June 2011

[9]. Atri Sanyal, and Amitabha Sinha. "Trans_Proc: A Reconfigurable Processor to Implement the Linear Transformations." IJSI vol.10, no.1 2022: pp.1-16.

[10]. Po-Chih Tseng et al, “Reconfigurable discrete cosine transform processor for object-based video signal processing”, in ISCAS '04. Proceedings of the 2004 International Symposium on Circuits and System, 2004.

[11]. Po-Chih Tseng, Chao-Tsung Huang, Liang-Gee Chen, “ Reconfigurable Discrete Wavelet Transform Processor for Heterogeneous Reconfigurable Multimedia Systems”, Journal of VLSI signal processing systems for signal, image and video technology, 2005

[12]. K. Joe Hass David F. Cox , “ Transform Processing on a Reconfigurable Data Path Processor”, 7th NASA Symposium on VLSI Design 1998

[13]. Amitabha Sinha, Mitrava Sarkar, Soumojit Acharyya, Suranjan Chakraborty, “A Novel Reconfigurable Architecture of a DSP Processor for Efficient Mapping of DSP Functions using Field Programmable DSP Arrays”, ACM SIGARCH Computer Architecture News Vol. 41, No. 2, May 2013

[14]. P. S. Reddy, S. Mopuri and A. Acharyya, "A Reconfigurable High Speed Architecture Design for Discrete Hilbert Transform," in IEEE Signal Processing Letters, vol. 21, no. 11, pp. 1413-1417, Nov. 2014, doi: 10.1109/LSP.2014.2333745

[15]. S. K. Samaddar, A. Sanyal, "A Combined Architecture for FDCT Algorithm," Proc. 2012 Third International Conference on Computer and Communication Technology, Allahabad, 2012, pp. 33-37,doi: 10.1109/ICCCT.2012.16

[16]. Atri Sanyal, Swapan Kumar Samaddar, Amitabha Sinha , " A Generalized Architecture for Linear Transform" , Proc.IEEE International Conference on CNC 2010, Oct 04-05, 2010 , Calicut,Kerala, India , IEEE Computer society , pp.55-60 ,ISBN: 97-0-7695-4209-6

[17]. Atri Sanyal, Amitabha Sinha, "A Reconfigurable Architecture to Implement Linear Transforms of Image Processing Applications", International Conference on Frontiers in Computing and System (COMSYS 2020), Jalpaiguri, West Bengal, India, January 13-15,2020

[18]. Davide Rossi , Fabio Campi , Simone Spolzino , Stefano Pucillo , Roberto Guerrieri, "A Heterogeneous Digital Signal Processor for Dynamically Reconfigurable Computing", IEEE Journal of Solid-State Circuits ,Volume: 45, Issue: 8, Aug. 2010

[19]. Bin Zhang, Kuizhi Mei, Nanning Zheng, "Reconfigurable Processor for Binary Image Processing", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL. 23, NO. 5, MAY 2013