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Design of High-Speed Low Power Full Adder Using TFET

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ABSTRACT

A full adder circuit is considered as one of the fundamental building block for Digital Signal Processors (DSPs), Arithmetic and Logical Units (ALUs), Application Specific Integrated Circuits (ASICs) in VLSI design. So speed power and area are the three main design metrics for any VLSI circuits. The speed of the higher level design depends on the speed of full adder circuits. Thus realizing an efficient adder is required for better performance of an ALU and therefore the processor. A low power and high performance 1-bit full adder is proposed. In the existing system 8T NMOS full adder technique has been used. This NMOS full adder provides low speed and consumes more power. The major disadvantage is load capacitance effect. Compared to earlier designed NMOS full adder, the proposed TFET full adder shows a significant improvement in Power Delay Product (PDP), and speed. The simulation and power analysis are carried out using cadence virtuoso environment with 180 nm technology.

Keywords : Tunnel FET, Full adder, PTL(Pass Transistor Logic), Speed, Power, ALU(Arithmetic and Logical Unit),Transistor(T)

I. INTRODUCTION

Addition is the basic operation performed by the Arithmetic and Logical Unit. The parameters used for measuring the performance of VLSI circuits are speed power consumption and also cost. Power consumption of VLSI circuits must be reduced because the primary focus in VLSI design is to maximize the energy efficiency and speed. The power consumption plays a major role in modern equipment's due to the tremendous growth in handful electronic devices. Power efficient high performance circuits are looked-for any electronics gadgets. The supporting hardware should be equally inexpensive and compact. So, VLSI design engineers are now concentrating on power efficient designs to meet the critical design issues. The MOSFET technology is dominated in the past four decades for designing the VLSI circuits due to its desirable speed, power consumption and cost. Continuing scaling down in MOSFET devices leads to short channel effect, which is due to the leakage current. The scaling down of MOSFET will be end at 2026, when the size of the gates will be 5.9 nanometres long. It is quarter the length of the size they are today. There is a replacement is needed for the conventional MOSFETs. When the barrier size reduced in the MOSFET the electrons will tunnel through the barriers. But the Tunnel FET turns this phenomenon as advantage.

The MOSFET works by raising and lowering the height of the energy barrier. But the Tunnel FET works by changing the width of the energy barrier. The Tunnel FET has several advantages compared with the conventional MOSFETs. They are Consumes low power and low voltage, reduced short channel effects, reduction in the leakage current, good isolation between the drain and source, and also they have low subthreshold voltage swing (<60mV/decade) compared with ideal MOSFETs. The Tunnel FET works on the principle of electron tunneling.

In this paper, a low power and high-speed 1-bit full adder is proposed using Tunnel FET. The proposed adder is designed using Pass Transistor Logic (PTL), which eliminates the number of active transistors.

II. METHODS AND MATERIAL

1. Tunnel FET Structure

TFET utilizes the band to band tunneling as the conduction mechanism, which is an alternative for conventional MOSFETs. The basic Tunnel FET is similar to the structure of MOSFET except that the drain and the source are doped with opposite type of material. The common TFET structure consists of P-I-N (P-type Intrinsic N-type) structure. The intrinsic region is controlled by varying the potential of the gate terminal.

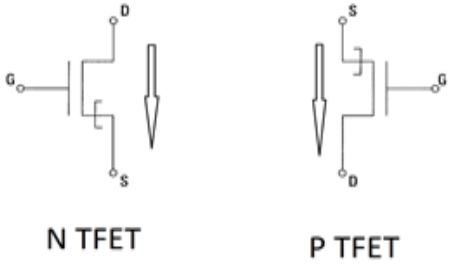

Figure 1: Symbol for n-TFET & p-TFET

The intrinsic region is controlled by varying the potential of the gate terminal.

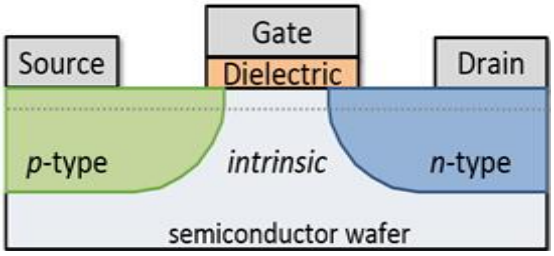

Figure 2: Basic TFET structure

The device is operated by applying gate bias voltage so that the electrons will accumulate at the intrinsic region.

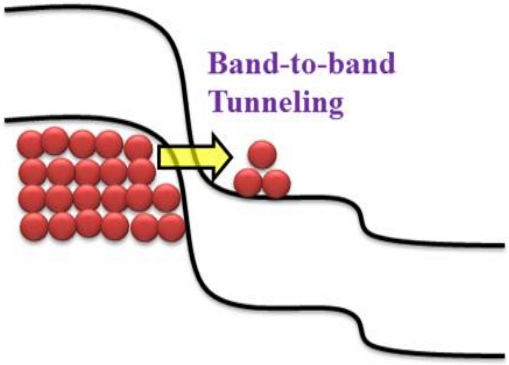

Figure 3: Tunneling process

The electrons have the ability to penetrate through the barriers a phenomenon called tunneling. When the required gate voltage is reached the band to band tunneling happens in the Tunnel FET.

2. Existing System

The several full adders were designed using static and dynamic logic styles. Among them the following adders were chosen for comparison. The 10-T SERF (Static Energy Recovery Full adder) is shown in figure 4. The SERF adder operates effectively at higher supply voltages. But at lower voltage supply the 10-T SERF is confronted with serious problems. When the A-pin is set to logic level "1" there will be a leakage current at the Cout-pin. The 8-T based full adder using 3-Transistor XNOR gate is shown in figure 5. This is a new approach for the full adder circuit which contain 2 XNOR gate and a multiplexer module. The delay is high in this adder circuit topology. Power dissipation is high in this circuit compared with other circuits. The NMOS 1-bit full adder circuit is implemented using pass transistor logic shown in figure 6, which uses Pass Transistor Logic style. This full adder circuit consumes less power compared with the other full adders. But the performance of the adder circuit configuration degrades when the load capacitance is increased above 400fF.

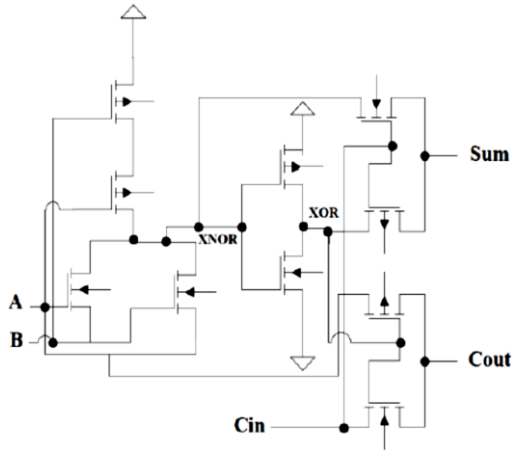

Figure 4 : 10-T SERF adder

In Pass Transistor Logic (PTL) the logics are realized using the serial and the parallel combination of connected Transistors. It reduces the number of transistors used to implement the logic function by reducing the number of active devices. so that the power consumption of this logic style is low. The speed also increased. In Pass Transistor Logic (PTL) they do not have a path from VDD to GND. There is no static power consumption in PTL. PTL has several advantages over the Domino logic and CMOS design. In PTL the low node capacitance provides very high speed. The reduced number of count of transistor leads to low power dissipation. Which in turn reduces the area of the circuits and also the interconnection.

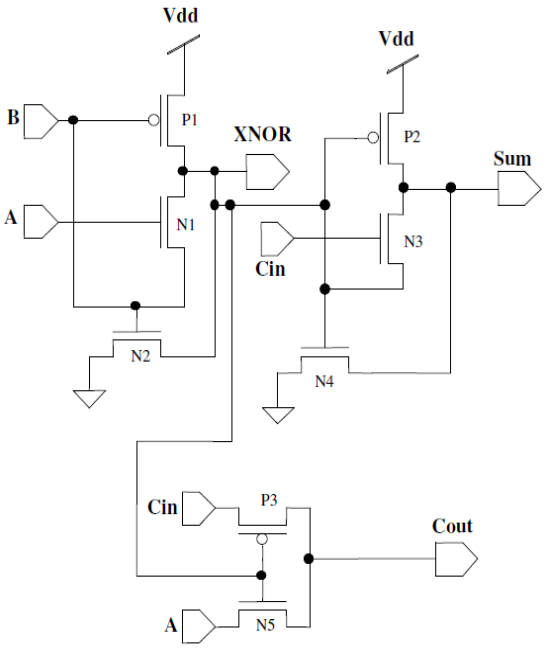

Figure 5: 8-T based full adder using 3-Transistor XNOR gate

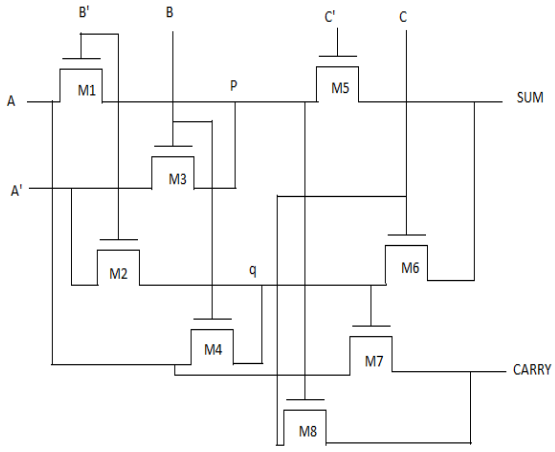

Figure 6: 1-Bit NMOS full adder

3. Proposed System

The proposed N-TFET based low power high speed 1-bit full adder has been designed using the PTL technique shown in figure 7.

The first transistor M1 is generating output AB´ while M3 is generating A´B. The two outputs together generate (A ⊕ B) at point p. Outputs of M2 and M4 are A´B´ and AB respectively. They produce (A⊙B) after meeting at point q. The logic at the outputs of M5 and M6 are (A ⊕ B) C´ and (A⊙B) C. They are generating the Sum output in the following manner:

Here Sum = A ⊕ B ⊕ C

And Carry = AB + BC + CA

= AB + BC (A+A´) + CA (B+B´)

= AB + ABC + A´BC + AB´C

= AB (1+C) + (AB´ + A´B) C

= AB + (A ⊕ B) C

Sum = (A ⊕ B) C' + (A ⊕ B)' C = A ⊕ B ⊕ C

Similarly, the output logics of M7 and M8, (A⊙B) A and (A ⊕ B) C, together generate Carry output as:

Carry = (AB) A + (A ⊕ B) C

= (AB + A´B´) A + (A ⊕ B) C

= A⊙B + (A ⊕ B) C

The proposed adder circuit has the sub threshold voltage swing less than 60mV/dec, which increases the circuit speed.

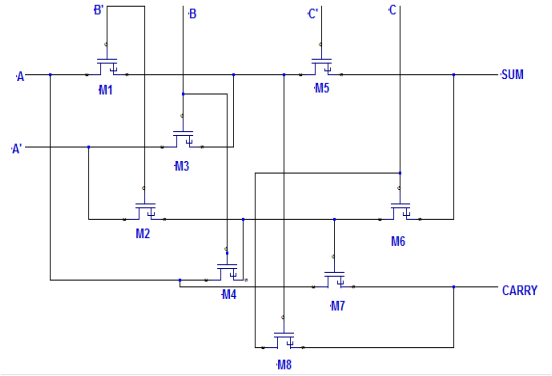

Figure 7: Proposed TFET full adder

III. RESULTS AND DISCUSSION

EXPERIMENTAL RESULTS

The proposed full adder circuit has been designed using 180um TFET technology. As the TFET circuits are in research side the inbuilt device models are not available so that the library files were created in cadence virtuoso platform. The input patterns were given to all full adder circuit was shown in table 1.

Table 1: Truth Table for full adder circuit

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The table 2 shows the truth table of the proposed adder circuit. The table 2 shows the power dissipation of the various full adder circuits. Various full adder circuits were compared with the proposed system and tested in same environment. Table 3 shows the power dissipation of various full adder circuits.

Table 2: Truth table for proposed full adder circuit

A	B	C	M1	M2	M3	M4	M5	M6	M7	M8	SUM	CARRY
0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	1	0	0	1	0
0	1	0	0	0	1	0	1	0	0	0	1	0
0	1	1	0	0	1	0	0	0	0	1	0	1
1	0	0	1	0	0	0	1	0	0	0	1	0
1	0	1	1	0	0	0	0	0	0	1	0	1
1	1	0	0	0	0	1	0	0	1	0	0	1
1	1	1	0	0	0	1	0	1	1	0	1	1

Table 3: Comparison of power consumption and number of transistors required of various adder configuration

Sl.no	Adder Configurations	Power Consumption(uW)	No.of Transistors
1	TGA20T	1255.54	20
2	16T adder	591.07	16
3	10T SERF adder	531.29	10
4	8T full adder	581.542	8
5	NMOS full adder	248	14
6	Proposed work	190.68	8

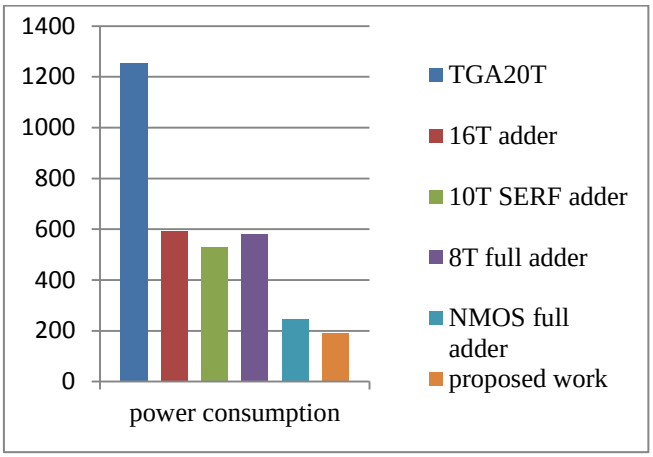

Figure 8 : power dissipation of various full adders.
Figure 8 shows the power consumption of various full adder circuits which are compared with the proposed system.

Table 4: Result analysis of NMOS and TFET full adder

Parameter	Existing system	Proposed system
Transistor count	14	8
Power(µW)	248µW	163.90µW
Delay	0.688 ns	0.3376ns
Voltage swing	63mV/dec	(34-45)mV/dec

The proposed system has the power consumption of 163.90uW

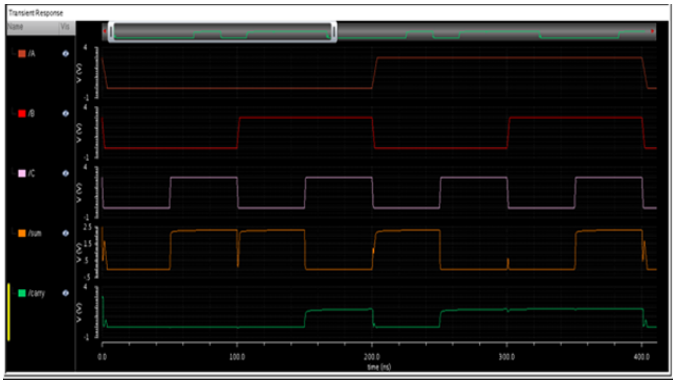

Figure 9 : simulated wave form of the proposed adder

The table 4 shows the result analysis of NMOS and TFET full adder circuit. The proposed full adder shows 66% power consumption and 49% time consumption than the NMOS full adder.

IV. CONCLUSION

A 1-bit full adder is designed using Tunnel FET Transistor based on PTL (Pass Transistor Logic). This reduces the number of active devices. The subthreshold voltage swing of the Tunnel FET is very lower than that of MOSFET (i.e.) <60mv/decade is possible in Tunnel FET. The factors such as speed and power consumption of the proposed adder is analysed and compared with different full adder circuits. The proposed full adder circuit consumes low power and provides high switching speed than the conventional MOS transistors.

As future work the different multiplier circuits are designed using the implemented Tunnel FET adder circuit. Among these multipliers which gives low power dissipation and high speed will be used for implemented on the FIR filters, DSP Processors, multiply and accumulate circuits.

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