International Journal of Scientific Research in Computer Science, Engineering and Information Technology
© 2017 IJSRCSEIT | Volume 2 | Issue 2 | ISSN : 2456-3307

Z-Source-Based Multilevel Inverter With Reduction

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ABSTRACT

A lot of roads in India have been in very bad shape Abstract: This study present a new inverter topology based on combination of cascaded basic units and one H-bridge component the essential component include single Z source, single DC voltage source and two switches generate two voltage level. The cascaded essential units produce positive and zero-voltage level and in the same time suggested inverter obtain positive, zero- and negative voltage levels, as a cause the add up to of power semiconductor switches is complete with esteem to established multilevel inverters. In this topology, production voltage amplitude is not boundless to DC sources voltage outline alike to traditional cascaded multilevel inverters and can be boosted with Z network shoot-through state control; consequently other DC/DC converters are not needed and it is more reliable against short circuit. Besides as compared with long-established Z-source inverter, total harmonic distortion of injected voltage is decreased in the optional inverter topology. The show of proposed topology and its controller are authorized with simulation results obtained using MATLAB/SIMULINK software and the power of the planned multilevel inverter-based Z source is obtained by result.

Keywords ; Seven-level multilevel, Z-source inverter, THD

I. INTRODUCTION

Power quality has been tracking down more responsiveness in recent years because of growth in by means of of industrial loads that are profound to power quality problems. Power quality problems can cause sensitive manufacturing equipment to operate in an irregular manner, prominent to issues with consistency of product and subsequent financial loss for the manufacturing organization. One of the most essential power quality issues is voltage instability such as sag and swell. Power quality studies show that 80 – 90% of the electrical customers' discontentment is because of voltage sags [1]. There are various way out to these problems, of which dynamic voltage restorer (DVR) is one of the most effective types. A DVR is mainly a controlled voltage source fixed between the supply and a sensitive load and it can inject a voltage on the system to pay off for any voltage disturbance in the distribution network. The compensation capability of a DVR depends on the maximum voltage injection capacity and active power which can be delivered by the DVR [2].

Energy storage devices such as battery or super conducting magnetic energy storage systems are required in DVR topology [2]. Due to the energy limitations of these sources, renewable sources are proposed.

Renewable sources such as solar or fuel cells can also be consumed as energy sources at the DC bus in renewable sources-fed DVR [3]. In the anticipated DVR design, a photovoltaic (PV) system with battery storage is merged to function as a DC voltage source. The electric power made by the PV system can be well thought-out economically viable. In the conventional PV assembly systems, the other converter as a DC – DC boost chopper is exploited to increase output DC voltage of the PV. In the recommended topology, Z-source Inverter is employed as a substitute of DC – DC boost chopper. The Z-source inverter consumes Z-impedance network between the DC supply and inverter circuitry to achieve boost operation [4]. The voltage boost is attained by given that a shoot- through state when both switches are in the same phase connection are on which is not possible with normal inverter topology [4–6].

The Z-source inverters in the associating of

old-fashioned inverters are lower costs, reliable, lower complexity and high efficiency [4 – 8].In modern years, the multilevel voltage inverter has received wide consideration in research and high-power applications such as huge induction motor drives, UPS systems and flexibl AC transmission systems [9].

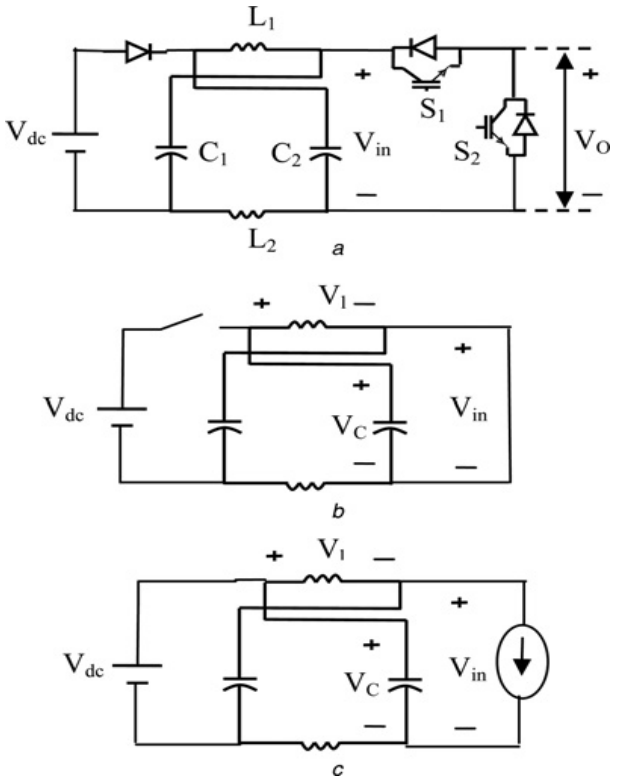

Figure 1. Circuit Diagram

1a Single-phase proposed basic unit
1b Simple unit in shoot-through state
Ic simple unit in non-shoot-through state

Multilevel inverter yields a preferred output voltage from several levels of input DC voltage sources. With an joint number of DC voltage sources, the inverter voltage output waveform slants approximately sinusoidal waveform but using a fundamental frequency switching order [10]. As related to outmoded two-level inverters, the multilevel inverters take more advantages, which devise lower semiconductor voltage stress, superior harmonic performance, small electromagnetic interference and minor switching losses [11,12]. The three collective topologies for multilevel inverter are as: (i) diode clamped (ii) flying capacitor and (iii) cascaded H-bridge inverters [13, 14]. Among them, a cascaded H-bridge inverter is suitable because it needs the reduced number of works to attain the similar amount of output voltage period between the conservative multilevel inverters [10]. However these advantages, extraordinary multilevel inverters vital the great number of power semiconductor switches. Recently, this problem has been solved in [15−17].

II. METHODS AND MATERIAL

A. Proposed Topology

Fig. 1a shows the recommended basic unit for a suggested topology. This includes of a DC voltage source, Z impedance with two switches S_1 and S_2. It can switch in two modes: non-shoot-through and shoot-through state. In the shoot-through state, both switches S_1 and S_2 are on and output voltage is zero. The equivalent circuit of shoot.

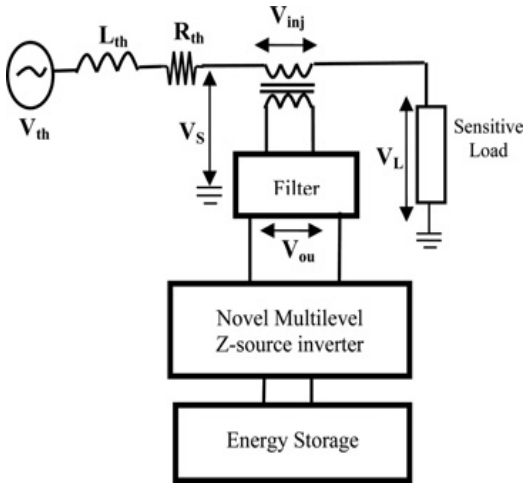

Figure 2. Block diagram of a DVR-connected sensitive load

The basic units shown in Fig. 2 can be corresponding together shown in Fig. 3a. In this paper PV arrays are expected to be the same, so all DC voltage sources are similar and shoot-through state times are equal in all units. The output voltage of this configuration can be expressed as

$$V_o = V_{o1} + V_{o2} + \cdots + V_{on}$$

TABLE 1 : SWITCHES STATES AND VO VALUE

State	ON switches	Output voltage (V_O)
1	S1	V_{in} (non-shoot through)
2	S2	0 (non-shoot through)
3	S1,S2	0 (shoot through)

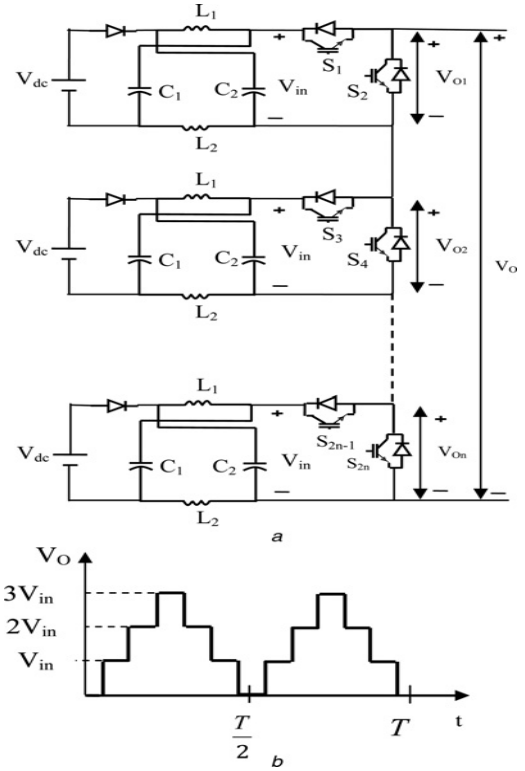

Figure 3. Cascaded proposed basic units
Fig.3a Configuration
Fig.3b Output voltage of four levels
Fig. 3b presents V_O for three basic units.

V_O has different levels such as 0, V_{in} , $2V_{in}$, . . . , nV_{in}.It is clear that V_O is just positive or zero, to generate a nearly waveform which approaches sinusoidal, final configuration is presented in Fig. 4 that full bridge is coupled to the cascaded basic unit in Fig. 3a. For $0 < t < (T/2)$, S_a , S_b are fired together and positive half of V_{ou} is generated, for $(T/2) < t < T$, S_c, S_d are on and negative half of output waveform is created. It is clear that period time of V_O is half of period time of V_{ou}

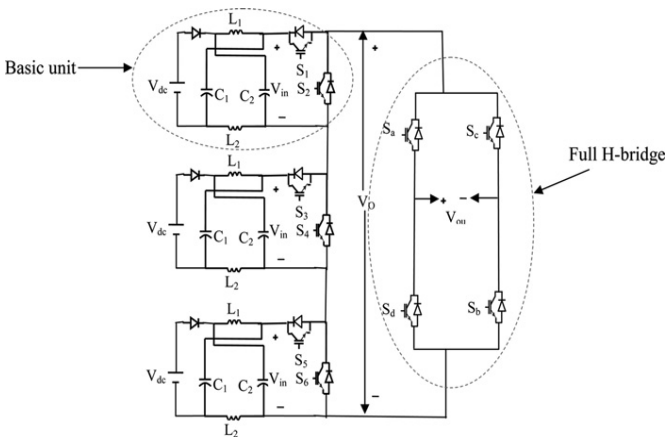

Figure 4. Seven-level multilevel inverter-based Z

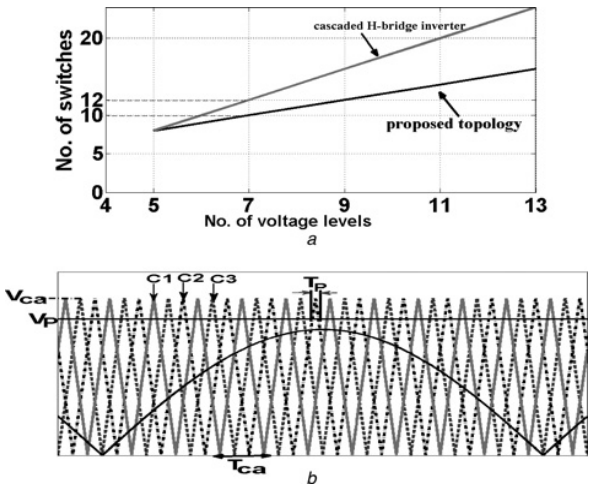

Figure 5. Required switches and switching algorithm

Fig.5a Comparison of the required switches to output voltage levels
Fig.5b switching algorithm of the proposed inverter

In the proposed topology, the maximum number of output phase voltage is given by

$$m = 2n + 1 \qquad (11)$$

n, m are the number of DC voltage source and the maximum number of levels of phase voltage, correspondingly. In the conventional cascaded multilevel inverter, the relation between the number of DC voltage source and the maximum number of levels of output phase voltage is similar to proposed topology. As a consequence, for the same number of output phase voltage, the number of DC voltage source is the equal.

The amount of power electronic switches (IGBTs and gate drives) in the single phase of recommended topology is given by

$$k = m + 3 \qquad (12)$$

Where k is the total number of switches.

In the conventional cascaded multilevel inverter the total number of power switches is given by

$$k = 2(m - 1)$$

(13) Fig. 5a associates the number of switches in the recommended Topology in this paper as shown in Fig. 4 with the conventional cascaded multilevel inverter.

As shown in this figure, the suggested topology needs less switches for realizing m voltages for output. This point reduces the setting up area and the number of the gate drives.

For example, to generate seven levels of output voltage (m ¼ 7), proposed topology needs only ten switches where conventional cascaded H-bridge multilevel inverter requires 12 switches. Numerous modulation strategies have been proposed for multilevel converters. Among these methods, the most common one used is the sinusoidal pulse-width modulation (SPWM). The principle of the SPWM method is based on a Evaluation of a sinusoidal reference waveform, with shifted carrier triangular waveforms.

Proposed switching algorithm for topology shown in Fig.3a where n ¼ 3, are revealed.

For the Z-source inverter the basic idea of control is to turnFig.5b. For each basic unit one triangle waveform with Period time of $T_{ca\ expected}$. This method procedures one straight line (Vp) to control the shoot-through stet time. Traditional zero states in to shoot-through states by possession unchanged the active switching states. Moreover, a proposed switching algorithm is recommended that generates shoot-through state during traditional zero states interval. Just levels of output voltage are boosted and configuration of output voltage is nearly like as conventional multilevel inverters output. As a consequence, the total harmonic distortion (THD) of output voltage is not more affected by Z source.

Respectively basic unit turns into shoot-through state when the related triangle waveform is superior to Vp and otherwise it operates just as traditional pulse-width modulation (PWM). For example, if C_1 carrier signal is lower than sinusoidal waveform then just S_1, in the connected basic unit is on and V_{o1} ¼ V_{in} , else if C_1 carrier signal is superior than sinusoidal waveform and lower than Vp then just S_2 is on and V_{o1} ¼ 0, else C_1 is greater than Vp, then S_1 , S_2 are on and basic unit is in the shoot-through state. Therefore boost factor of proposed inverter can be measured by the value of Vp..

B. Z-Sourcecomponent Design

During traditional operation mode the input voltage appears across the capacitor and no voltage appears across the inductor. During shoot-through time, the inductor voltage is same as capacitor voltage and inductor current increases linearly. The job of the inductor is to limit the current ripple during shoot-through state

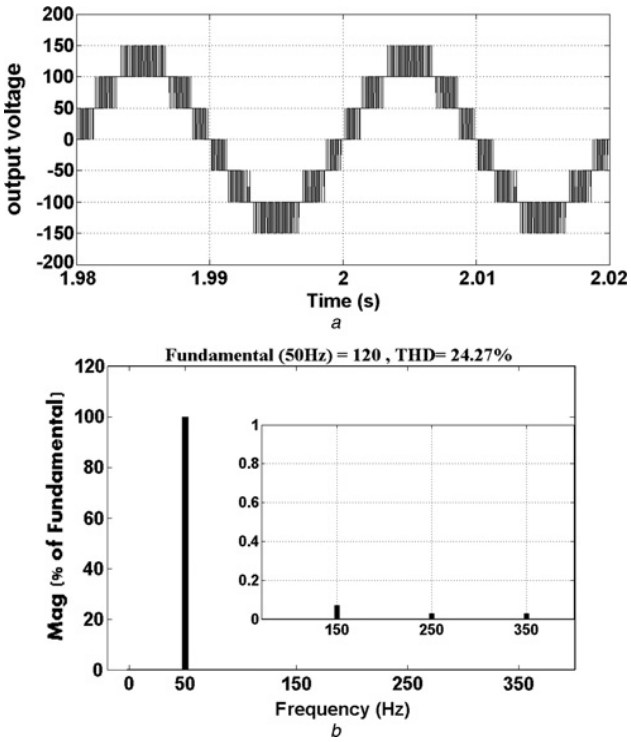

Figure 6. Conventional cascaded multilevel inverter (seven levels).

Modulation index and DC voltage sources. Figs. 8a and b existing load voltage and harmonic spectrum of load voltage in nine levels conventional cascaded multilevel inverter. It is measured that THD of output voltages for proposed topology and conventional cascaded multilevel inverter almost are the same. In order to display the performance of proposed DVR in voltage sag mitigation, the DVR based suggested inverter shown in Fig. 4 is simulated. The system parameters are registered in Table 3.

It is assumed that the voltage magnitude of the load must be set at 1 pu during the voltage disturbance. A case of voltage sag with 20% depth and duration of 100 ms is initiated at t ¼ 0.2 as shown in Fig. 6a. The DVR can compensate for the dropped voltage immediately. Figs. 6b and c show the DVR-injected voltage and sensitive load voltage, respectively. Fig. 6d shows inverter output phase voltage (Vou). B is appointed with control unit of DVR about 5.33.

III. RESULTS AND DISCUSSION

A projected single-phase multilevel inverter-based Z source was built by means of IRFP460 MOSFETS as the switching devices and MUR820G as fast diodes in the Z-source topology. A DC voltage source with amplitude 10 V was used to independently supply of each basic units. Z networks consist of 630 mf capacitors and 2.2 MH inductors.

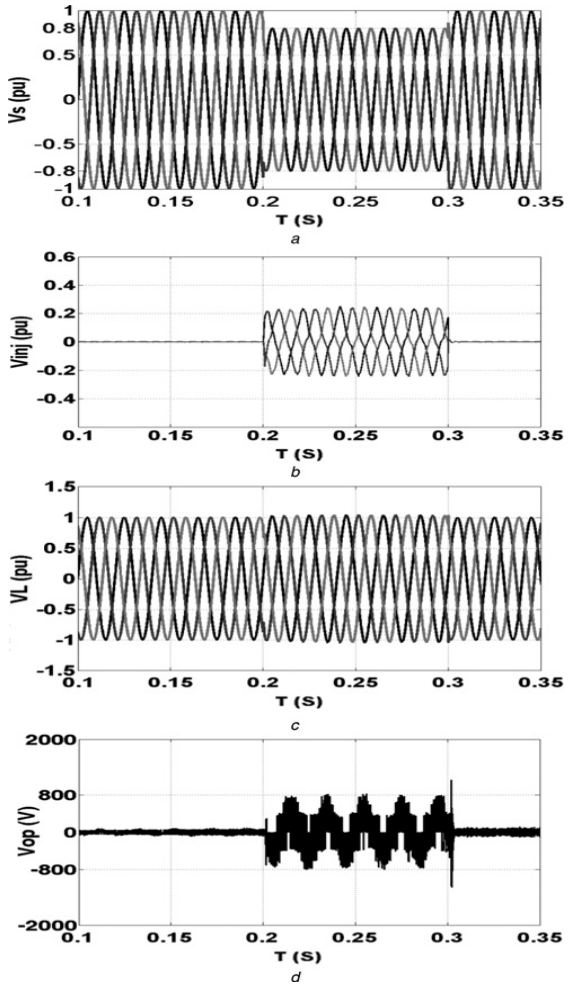

Figure 7. Balanced Voltage Sag

Prototype was configured to effort as a five-level inverter. The switching signals which were obtained from the proposed PWM algorithm were produced with microcontroller for B ¼ 1.25 and f ¼ 50 Hz. The switching signals were interfaced to the inverter power switches concluded opt coupler isolators TLP521. Fig. 10a shows snapshots of the prototype. It consists of two simple units, two Z-source networks, two DC voltage sources, one full bridge, load (72 + 11.3j V) and a microcontroller.

During traditional operation mode the input voltage appears across the capacitor and no voltage appears across the inductor (just a pure DC current flow through the inductors). During shoot-through time, the inductor voltage is same as capacitor voltage and inductor current increases linearly. The job of the inductor is to limit the current ripple during shoot-through state.

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IV. CONCLUSION

In this study, the modelling and simulation of a DVR with a novel multilevel-based Z-source inverter have been shown. The proposed inverter has less switches as related to a traditional cascaded multilevel inverter. Suggested inverter increases DVR compensation capability and reliability via Z-source inverter characteristics, Simulation and experimental effects show the ability of the proposed inverter. The simulation consequences show that the compensates for the voltage disturbances such as sag and swell quickly and delivers excellent voltage regulation.

V. REFERENCES

[1]. Choi, S.S., Wang, T.X., Mahinda Vilathgamuwa, D.: 'A series compensator with fault current limiting function', IEEE Trans. Power Deliv., 2005, 20, (30), pp. 2248 – 2256

[2]. Banaei, M.R., Hosseini, S.H., Khanmohamadi, S.,Gharehpetian, G.B.:'Verification of a new energy control strategy for dynamic voltage restorer by simulation', Elsevier J. Simul. Model. Pract. Theory, 2006,14, (2), pp. 112 – 125

[3]. Hanif, A., Choudhry, M.A.: 'Investigation voltage restoration and power export in a

distribution system with series compensator using distributed generation', Arab. J. Sci. Eng., 2010, 35, (1B), pp. 265 – 291

[4]. Shen, M., Joseph, A., Wang, J., Peng, F.Z., Adams, D.J.: 'Comparison of traditional inverters and Z-source inverter for fuel cell vehicles', IEEE Trans. Power Electron., 2007, 22, (4), pp. 1453 – 1463)

[5]. Shen, M., Hodek, S., Peng, F.Z.: 'Control of the Z-source inverter for FCHEV with the connected to the motor neutral point'. Power Electronics Specialists Conf., PESC, 2007

[6]. Wang, J., Peng, F.Z., Tolbert, L.M., Adams, D.J.: 'Maximum constantboost control of the Z- source inverter'. Industry Application Conf.,39th Annual Meeting Conf. Record, 2004

[7]. Das, A., Lahiri, D., Dhakar, A.K.: 'Residential solar power systems using Z-source inverter'. IEEE Regional 10 Conf., TENCON,2008

[8]. Das, A., Chowdhury, S., Chowdhury, S.P., Domijan, A.: 'Performance analysis of Z-source inverter based ASD system with reduced harmonics'. Power and Energy Society General Meeting –Conversion and Delivery of Electrical Energy in the 21st Century, Pittsburgh, July 2008

[9]. Al-Othman, A.K., Abdelhamid, T.H.: 'Elimination of harmonics in multilevel inverters with non-equal dc sources using PSO', Elsevier Energy Convers. Manage., 2009, 50, pp. 756 – 764

[10]. Park, S.-J., Kang, F.-S., Cho, S.E., Moon, C.-J., Nam, H.-K.: 'A novel switching strategy for improving modularity and manufacturability of cascaded-transformer-based multilevel inverters', Elsevier Electr.Power Syst. Res., 2005, 74, pp. 409 – 416

[11]. Corzine, K.A., Wielebski, M.W., Peng, F.Z., Wang, J.: 'Control of cascaded multilevel inverters', IEEE Trans. Power Electron., 2004,19, (3), pp. 732 – 738

[12]. Barkati, S., Baghli, L., Berkouk, E.L.M., Boucherit, M.-S.: 'Harmonic elimination in diode-clamped multilevel inverter using evolutionary algorithms', Electr. Power Syst. Res., 2008, 78, pp. 1736 – 1746

[13]. Rodriguez, J., Lai, J., Peng, F.Z.: 'Multilevel inverters: a survey oftopologies, controls, and applications', IEEE Trans. Ind. Appl., 2002,49, (4), pp. 724 – 738

[14]. Selvaraj, J., Rahim, N.A.: 'Multilevel inverter for gird – connected PVsystem employing digital PI controller', IEEE Trans. Ind. Electron.,2009, 56, (1), pp. 149 – 158

[15]. Banaei, M.R., Dehghanzadeh, A.R.: 'A novel Z-source based multilevel inverter for renewable sources fed DVR'. Power Quality Conf. (PQC),Tehran, Iran, 2010

[16]. Babaei, E., Hosseini, S.H.: 'New cascaded multilevel inverter topology with minimum number of switches', Energy Convers. Manage., 2009,50, pp. 2761 – 2767

[17]. Banaei, M.R., Salary, E.: 'New multilevel inverter with reduction of switches and gate driver', Energy Convers. Manage., 2011, 52, pp. 1129 – 1136

[18]. Hanif, M., Basu, M., Gaughan, K.: 'Understanding the operation of aZ-source inverter for photovoltaic application with a design example',IET Power Electron., 2009, 4, pp. 278 – 287