International Journal of Scientific Research in Computer Science, Engineering and Information Technology
© 2018 IJSRCSEIT | Volume 3 | Issue 1 | ISSN : 2456-3307

Design and Verilog HDL Implementation of Carry Skip Adder Using Kogge-Stone Tree Logic

K. Reshma Priyanka[1], A. M. Gunasekhar[2]
[1]M.Tech Student, Department of ECE, Sree Rama Institute of Technical Education, Tirupathi, India
[2]HOD & Associate Professor, Department of ECE, Sree Rama Institute of Technical Education, Tirupathi, India

ABSTRACT

The portable equipment's such as cellular phones, Personal Digital Assistant (PDA), and notebook personal computer, arise the need of effective circuit area and power efficient VLSI circuits. Addition is the most common and often used arithmetic operation in digital computers and also, it serves as a building block for synthesis all other arithmetic operations. In this paper, we present a carry skip adder (CSKA) structure that has a higher speed yet lower energy consumption compared with the conventional one. The speed enhancement is achieved by applying concatenation and incrementation schemes to improve the efficiency of the conventional CSKA (ConvCSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both fixed stage size and variable stage size styles, wherein the latter further improves the speed and energy parameters of the adder. The proposed method uses compound gates such as AOI and OAI as skip logic in the design that leads to decrease area usage, delay and power consumption, also in addition the parallel prefix kogge stone adder is included to attain further reduction of power. The design is coded in Verilog HDL and its simulation, area, delay and power are analyzed using Xilinx_ISE 14.3.

Keywords : Carry skip adder, AND-OR-Invert logic, KoggeStone adder, hybrid variable latency adders.

I. INTRODUCTION

The binary adder is the critical element in most digital circuit designs including digital signal Processors (DSP) and microprocessor data path units. Such, extensive research continues to be focused on improving the power delay performance of the adder. In the VLSI implementations parallel-prefix adders are known to have the best performance. Reconfigurable logic such as Field Programmable Gate Arrays (FPGAs) has been gaining in popularity in recent years because it offers improved performance in terms of speed and power over DSP-based and microprocessor-based solutions for many practical designs involving mobile DSP and telecommunications applications and a significant reduction in development time and cost over Application Specific Integrated Circuit (ASIC) designs. The power advantage is especially important with the growing popularity of mobile and portable electronics, which make extensive use of DSP functions. However, because the structure of the configurable logic and routing resources in FPGAs, parallel-prefix adders will have a different performance than VLSI implementations. In particular, most modern

FPGAs employ a fast carry chain which optimizes the carry path for the simple Ripple Carry Adder (RCA).

The addition operations will result in sum value and carry value. The Half Adders (HA) and Full Adders (FA) is the basic block of all adder architectures. There are several many adder families. These all having various delays, powers and area usages. Examples include ripple carry adder (RCA), carry increment adder (CIA), carry select adder (CSLA), carry skip adder (CSKA) and parallel prefix adders (PPAs).The Ripple carry adder has the simplest structure with the low power consumption and smallest area but with the worst critical path delay. In the CLSA, the speed, power consumption, and area usages are considerably larger than those of the RCA. The parallel prefix adder, it is also called carry look-ahead adders, that provide the direct parallel prefix structures to generate the carry as fast as possible. The CSKA, which is an efficient adder in terms of power consumption and area usage, was introduced .The CSKA has much smaller critical path delay than the one in the RCA, whereas its area and power consumption are similar to those RCA. In this paper, we propose a modified structure for high speed carry skip adder. The conventional CSKA uses a 2:1 multiplexer for skip logic.

II. LITERATURE SURVEY

Kantabutra V.,[7] described a method for designing optimum-speed one-level carry skip adders. The one-level carry skip adder is designed with an optimum speed by a method that yields a fastest adder if the ripple time (a circuit parameter) of a carry signal is a linear function of the number of bit positions that the carry signal propagate through, and if the skip time (another circuit parameter) of a carry signal is a linear function of the number of blocks of bit positions skipped by the signal, or if these two parameters are such mildly non-linear functions that they can be modeled by a linear function without any effect on any of the results obtained. In this paper, delay reduced based on skip logic in single level but increase in area, excess power consumption and also less regular layout.

Chirca et al K.,[3] compared a carry skip adder by various existing logic styles. The most timing critical part of logic design usually contains one or more arithmetic operations, in which addition is commonly involved. In VLSI applications, area, delay and power are the important factors which must be taken into account in the design of a fast adder. The carry-skip adder reduces the time needed to propagate the carry by skipping over groups of consecutive adder stages, is known to be comparable in speed to the carry look-ahead technique while it uses less logic area and less power. In this, a design of 8-bit carry skip adder by various existing logic styles are to be compared quantitatively and qualitatively by performing detailed transistor-level simulation. In this paper, lower propagation delay and high performance but requires more area and large power consumption.

Alioto M. and Palumbo G.,[1] proposed a carry skip adder design for the achievement of minimum delay with the following two steps. One is a timing consideration based sizing in an analytical way and next is to attain a desired number of bits by a successive refinement. This paper, high performance and minimal circuitry is produced but having high critical path delay.

Milad Bahadori, Mehdi Kamal and Ali Afzali-Kusha,[8] presented a structure of carry skip adder with a high speed and low power consumption. In many of the works only the speed is considered as an important parameter rather than the area usage and the power consumption. The multiplexers that acting as a skip logic provides a large critical path delay even though it has a faster speed. The conventional carry skip adder having an optimum structure and it provides a better performance with the skip logics. But in the skip logic multiplexer is used, which reveals a large portion of critical path delay and the 2:1 multiplexer containing 12 transistors that leads to increase in area usage and power consumption.

III. CARRY SKIP ADDER

The carry skip adder comes under the category of a by-pass adder and it uses a ripple carry adder for an adder implementation. The formation of carry skip adder block is attained by improving a worst-case delay. The carry skip adder has a critical path, that passes through all adders and stops at the sum bit but actually it starts at first full adder. This adder is an efficient one according to its area usage and power consumption. The structure of 4 bit carry skip adder is shown in fig.1.

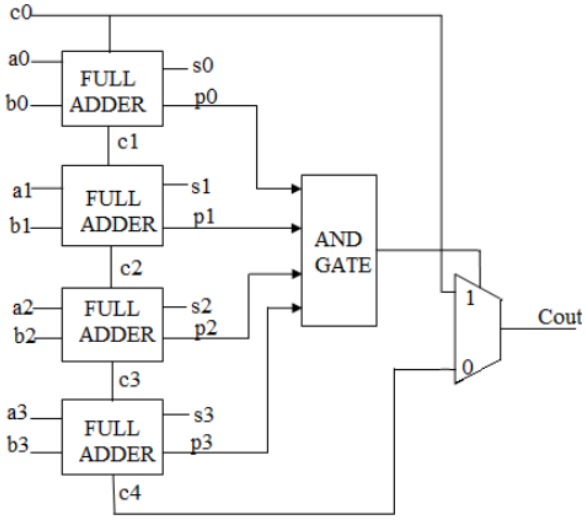

Figure 1 : Four bit carry skip adder

In CSKA the wiring lengths is short and also having a simple and regular layout because of the smaller number of transistors. Since it has lower speed, it is not used in high speed applications. This becomes a limitation.

IV. CONVENTIONAL CARRY SKIP ADDER

The CSKA structure in conventional form having stages that includes full adder chains, block of RCA and 2:1 multiplexer, this multiplexer acts as a skip logic. Through this multiplexers, RCA blocks are connected each other, this is placed at one or more structure-level.

The input of the multiplexer are the carry input of the stage and the carry output of its RCA block and the product of propagation signals is used as the selector signals of the multiplexer. The carry skip adder may be implemented using FSS and VSS where the highest speed may be obtained for the VSS structure. There may be a great impact on speed in a CSKA configuration. Based on a single-level carry skip logic, techniques generated may use variable stage size in order to minimize the delay. In some methods to increase the speed of the circuit multilevel

CSKA"s are proposed. Thearea and power increased considerably in this technique and having less regular layout.

The A and B are the input bits, that are given normal to the ripple carry adder along with the full adder chain and initial carry that should be zero (i.e. Ci = 0) and as a produced form to the input of the multiplexer. In multiplexer the select lines are chosen according to the carry output of the ripple carry adder and the final output of sum and carry are obtained from ripple carry adder and multiplexer respectively. Generally, carry skip adder is a form of by-pass adder and it uses a ripple carry adder as an adder implementation. The multiplexer used in the circuit acts as a skip logic, that skip logic is a logic flow and it is a branching of condition, a custom path is created through the certain condition views that may varies based on a respondent answer.

In the conventional carry skip adder the skip logic with multiplexer reveals a large portion of critical path delay. The 2:1 multiplexer containing 12 transistors that leads to increase in area usage and power consumption. So these are to be considered as drawbacks of the existing design.

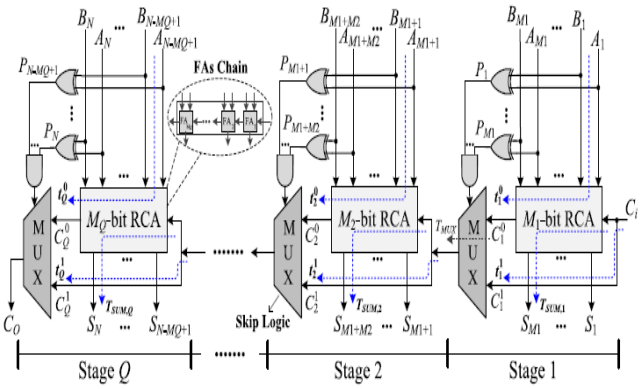

Figure 2 : Structure of conventional CSKA

V. CI-CSKA DESIGN

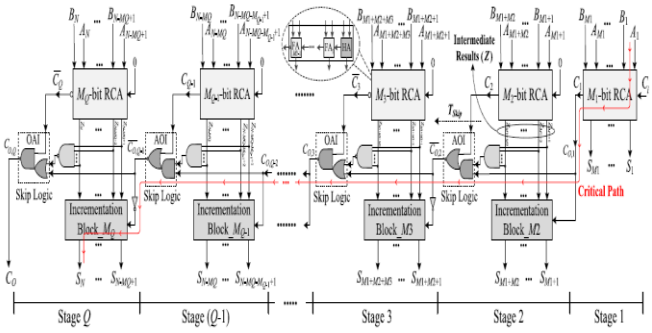

Figure 3 : Structure of CI-CSKA

The main objective of the proposed method is to enhance the speed and to improve the efficiency of the conventional carry skip adder. Have to reduce the power consumption of the design without impacting the speed of it and also have to reduce the area and critical path delay. In existing method due to the usage of multiplexer that acts as skip logic May leads to a large critical path delay and area usage and also a large power consumption. These drawbacks are going to be solved in the proposed design by using compound gates instead of multiplexer.

The AOI (AND-OR-Inverter) and OAI (OR-AND-Inverter) are called as compound gates, they acts as a skip logic in order to decrease the area usage and delay of the skip logics in conventional method. There is a reason behind the usage of both the AOI and OAI gates, these are generally called as compound gates as a skip logic is its inverting function of these gates in a standard cell libraries. Because of this usage of inverter gates the incrementation of power consumption and delay are eliminated.

VI. KOGGE STONE CSKA DESIGN

As mentioned in above section the speed of the normal carry skip adder improved by using incrementation and concatenation methods. The

proposed work is also using these methods. Reducing the skip logic delay may reduce the overall propagation delay. The proposed system introduces the parallel prefix network to reduce the delay in variable latency CSKA.

In prior work Brent-Kung adder is used for the parallel prefix network. In addition to this several parallel prefix, adders are there, Kogge-Stone adder, Han-Carlson adder and Lynch-Swartzlander spanning tree adder. In the proposed system, we use the Kogge-Stone adder. It is a parallel prefix form carry look-ahead adder. It is the fastest adder when compared to Brent-Kung adder. For this reason, we choose this adder for proposed work

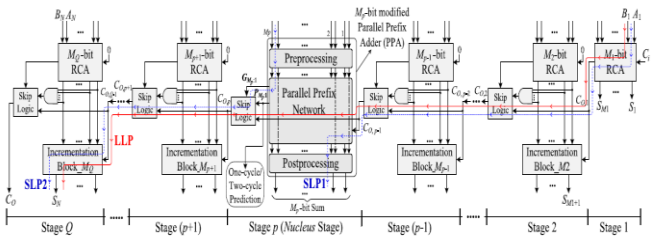

Figure 4 : Structure of Modified CSKA

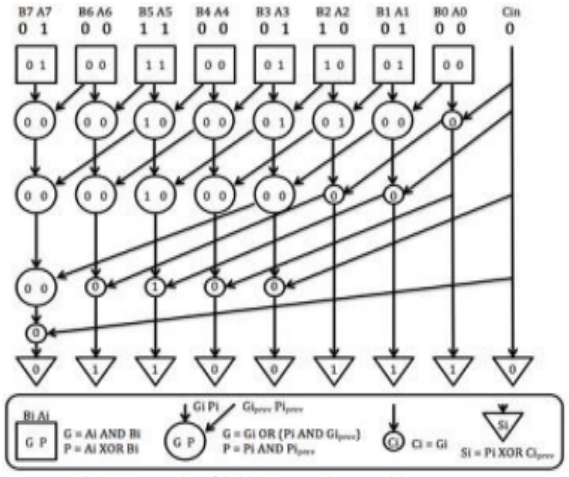

Figure 5. Example of 8-bit Kogge-Stone adder structure

For the proposed work parallel prefix network is included in between the stages of RCA as shown in Fig.3. This parallel prefix network combined with processing units is referred to as nucleus stage. The modified CSKA structure with parallel prefix network is shown in Fig.4. In this structure consist of two processing networks and parallel prefix adder network. The processing networks are used for different purposes. First one is used for pre-processing step and the second one is used for post-processing step. An input from the second RCA block is given to the parallel prefix network and the output of this network is fed to the third RCA network. This is a main modification in the proposed system.

The critical path from the first stage of RCA to last stage of RCA is termed as Long latency path (LLP). The path from the first stage of RCA to post processing network is termed as Short latency path 1 (SLP1) and the path from preprocessing unit to the last stage of RCA is termed as Short latency path 2 (SLP2).These two paths are considered for a calculation of critical path in the overall structure.

There are different types of parallel prefix structure namely, Brent-Kung adder, Han – Carlson adder, LynchSwartzlander, and Kogge-Stone adder. In the previous case, Brent-Kung adder is used but it has a drawback such as fan-out problems. Here in our proposed system, we use Kogge stone adder. The Kogge-stone adder was developed by Peter M. Kogge and Harold S. Stone. This is one type of parallel prefix adder. It has lower fan-out problems compared with other parallel prefix adders (PPAs). Fig.5. shows the example of 8 bit Kogge –stone adder. In this structure, each vertical stage generates a propagate and generate outputs.

The carries are generated vertically and these output bits are XOR'd with the initial propagate bits after the input to produce the sum output.

This is a more efficient adder especially the power consumption of this adder is significantly low when compared to other adders. As shown in below adder the carry input is given into first vertical stage, this first stage performs the XOR'd operation. A carry may be considered as 0 or 1.In this example, it is taken as 0.

The functioning of Kogge-Stone adder (KSA) is divided into three parts. These are1) Pre-processing, 2) Carry look ahead network, 3) Post processing. In a Pre-processing step, propagate and generate signal bits are generated for the pair input bits A and B.

$$Pi = Ai \text{ XOR } Bi$$
$$Gi = Ai \text{ AND } B$$

A carry look ahead block differentiates Kogge-Stone adder from others. This is the main difference to make this adder has more high performance. This step produce carries for each bit and it uses group propagate and generates given by the equations,

$$Pi:j = Pi:k+1 \text{ AND } Pk:j$$
$$Gi:j = Gi:k+1 \text{ OR } (Pi:k+1 \text{ AND } Gk:j)$$

Post processing is the final step of this KSA and it is also common to all adders of this carry look ahead families. Sum bits are generated by using below equation

$$Si=Pi \text{ XOR } Ci-1$$

Kogge-Stone adder is widely used adder because it generates carry in O (logn) time. In more industries, this adder is used for high performance.

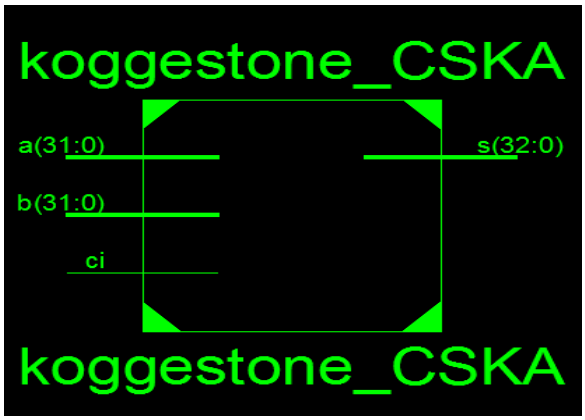

Figure 6. Block diagram

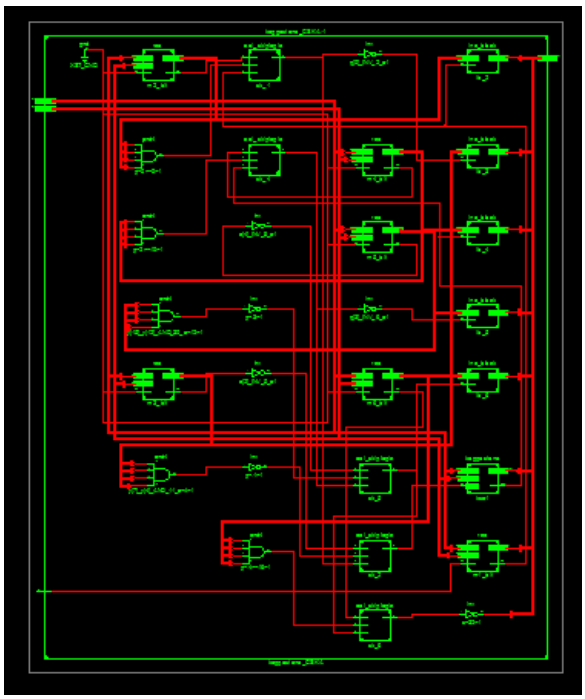

Figure 7. RTL schematic diagram

VII. RESULTS

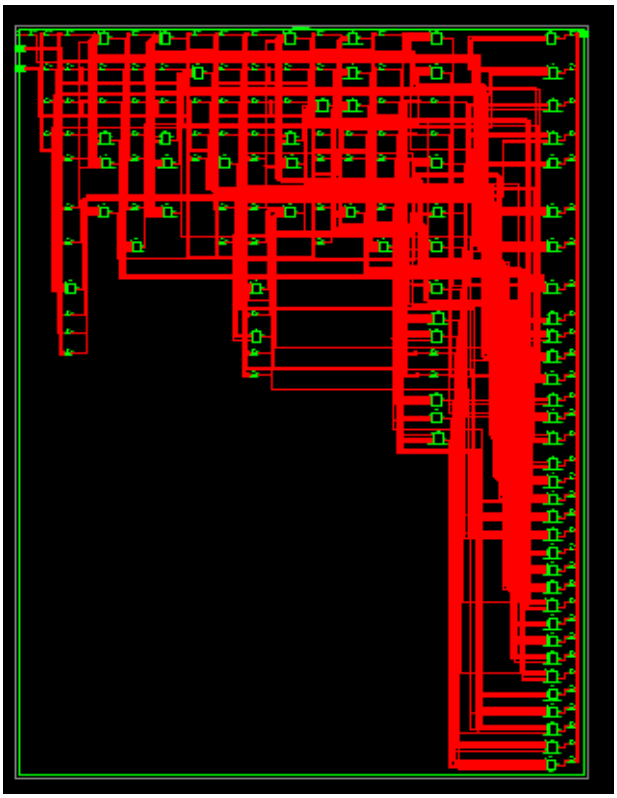

Figure 8: Technology schematic diagram

Different CSKA's	LUT's	IOB's	Delay(ns)
Conv-CSKA	72	98	15.386
CI-CSKA	75	98	10.731
Brent Kung CSKA	68	98	10.112
Kogge Stone CSKA	68	98	9.781

Table 1: comparison of different CSKA adders

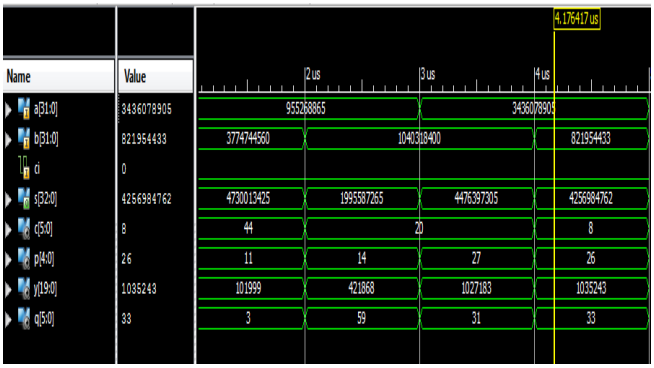

Figure 9 : Simulation results

VIII. CONCLUSION

In this paper, a structure called modified high speed carry skip adder (CSKA) was proposed. The main advantage of this paper is its ability to add two inputs with minimum delay time. This reduction in delay time can be achieved by using a parallel prefix adder network (PPA). This parallel prefix adder is inserted in the middle stages of RCA chain. The Kogge-Stone adder is used for this parallel prefix network. In addition to this, the power consumption of this structure is reduced by using AND-Or-Invert and Or-And-Invert gates for skip logics. An incrementation scheme increases the speed of the structure. These two modifications make this kogge stone carry skip adder more efficient.

IX. REFERENCES

[1]. M. Alito and G. Palumbo, "A simple strategy for optimized design of one-level carry-skip adders," IEEE Trans. Circuits Syst. I, Fundam. Theory. Appl., Vol. 50, no. 1, pp. 141-148, Jan. 2003.

[2]. Y. Chen, H. Li, J. Li and C. K. Koh, "Variable-latency adder (VL-adder): New arithmetic circuit design practice to overcome NBTI", in Proc. ACM/IEEE Int. Symp. Low Power Electron. Design (ISLPED), Aug. 2007, pp. 195-200.

[3]. K. Chirca et al., "A static low-power, high-performance 32-bit carry skip adder", in Proc. Euromicro Symp. Digit. Syst. Design (DSD), Aug./Sep. 2004, pp. 615- 619.

[4]. K. Du, P. Varman and K. Mohanram, "High performance reliable variable latency carry select addition", in Proc. Design Autom., Test Eur. Conf. Exhibit. (DATE), Mar. 2012, pp. 1257-1262.

[5]. S. Ghosh and K. Roy, "Exploring high-speed lowpower hybrid arithmetic units at scaled supply and adaptive clock-stretching", in Proc. Asia South Pacific Design Autom. Conf. (ASPDAC), Mar.2008, pp. 635-640.

[6]. S. Jia et al., "static CMOS implementation of logarithmic skip adder", in Proc. IEEE Conf.

Electron Devices Solid-State Circuits, Dec. 2003, pp. 509-512.

[7]. V. Kantabutra, "Designing optimum one-level carryskip adders", IEEE Trans. Comput., Vol. 42, no. 6, pp. 759-764, Nov. 1993.

[8]. Milad Bahadori, Mehdi Kamal and Ali AfzaliKusha,"„High-speed and energy efficient carry skip adder operating under a wide range of supply voltage levels", IEEE Transaction on Very Large Scale Integration (VLSI) Systems, 2015, Vol. 67, no. 4, pp. 324-335.

[9]. V. G. Oklobdzija, B. R. Zeydel, H. Dao ,S. Mathew, and R. Krishnamurthy, "Energy-delay estimation technique for high-performance microprocessor VLSI adders", in proc. 16th IEEE Symp. Comput. Arithmetic, Jun. 2003, pp.272-279.

[10]. N.Kaveri, P.Senthil Kumar, "An Efficient Architecture of Carry Select Adder using Logic Formulation", International Journal of Science and Research(IJSR), Vol 5, no.2, pp. 1444-1447, Feb 2016.

[11]. B.Ramkumar and H. M. Kittur, "Low-power and areaefficient carry select adders", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 20, no. 2, pp. 371-375, Feb. 2012.

[12]. R. Zlatanovici, S. Kao, and B. Nikolic, "Energy-delay optimization of 64-bit carry-lookahead adders with a 240 ps 90 nm CMOS design example", IEEE J. SolidState Circuits, Vol. 44, no. 2, pp. 569-583, Feb. 2009.