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High-Speed and Low Delay Parallel Prefix Adder with Skip Logic

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ABSTRACT

A carry skip adder (CSKA) structure is presented which has lower power consumption with a higher speed. The performance of the conventional CSKA is improved by achieving the speed enhancement by applying concatenation and incrementation schemes. The existed structure utilizes AND-OR-INVERT (AOI) and OR-AND-INVERT (OAI) compound gates for the skip logic. Low power very large scale integration (VLSI) circuits are most significant for designing of high performance and portable devices. The high speed, small area and low cost are the main considerations of VLSI circuits. This paper presents the design and hardware implementation of Hybrid variable latency CSKA. The proposed design is simulated using ISE simulator. The design shows 38% improvement in speed and 11.53% improvement in area compared to carry look ahead adder. The maximum power consumption for proposed system is 0.014W.

Keywords : Serial Adder, Parallel Prefix Adder, Kogge Stone Adder, High speed VLSI.

I. INTRODUCTION

VLSI Integer adders are applicable in Arithmetic and Logic units (ALU"s), microprocessors and memory addressing units. Speed of the adder often decides the minimum clock cycle time. Parallel Prefix adder is utilized for its speed when compared with ripple carry adder. Parallel Prefix adders have been established as the most efficient circuits for binary addition. The regular structure and fast performance of parallel prefix adder makes particularly attractive for VLSI implementation. The classical parallel prefix adder structures presented in the literature over the years optimize for logic depth, area, and fan-out and interconnect count of logic circuits. Parallel Prefix adders (PPA) are family of adders derived from the commonly known carry look ahead adders. The parallel prefix adders are KS adder (kogge-stone), SKS adder (sparse kogge-stone), Spanning tree and Brent Kung adder. These adders are flexible and used to speed up the binary additions. RCA is a serial adder. RCA is used to perform any number of additions.

RCA is serial adder and it has propagation delay problem. When bits are increasing then delay also increases simultaneously. Hence parallel adders (parallel prefix adders) are preferred in proposed system. RCA is replaced by Kogge Stone Adder (KSA) for increasing the speed with reduced area. The advantage of utilizing the flexibility in implementing the three structures based upon throughput requirements. Due to continuing integrating intensity and the growing needs of portable devices, low-power and high-performance designs are of prime importance.

II. PARALLEL PREFIX ADDER

The Parallel Prefix adders involve the execution of an operation in parallel. This is done by segmentation the operation in smaller pieces which are computed in parallel. The output is depends on the initial inputs. Parallel Prefix Adder (PPA) is equivalent to carry look ahead adder (CLA). A Carry look ahead adder is a type of adder used in digital logic. CLA is designed to overcome the latency

introduced by repelling effect of carry bits in RCA. A CLA improves speed by reducing carry bits. It calculates one or more carry bits before the sum, which reducethe wait time to calculate the result of larger bit value.

CLA uses the concept of generating (G) and propagating (P) carries. The two differ in the way their carry generation block is implemented. The main advantage of PPA is the carry reduces the number of logic levels by essentially generating the carries in parallel. PPA fastest adder with focus on design time and is the choice for high performance adder in industry. In this paper, design and implementation of optimized 32 bit KSA is proposed.

III. EXISTED SYSTEM

A.MODIFYING CSKAS FOR IMPROVING SPEED:

Alioto and Palumbo propose a simple strategy for the design of a single-level CSKA. The method is based on the VSS technique where the near-optimal numbers of the FAs are determined based on the skip time (delay of the multiplexer), and the ripple time (the time required by a carry to ripple through a FA).

The goal of this method is to decrease the critical path delay by considering a non integer ratio of the skip time to the ripple time on contrary to most of the previous works, which considered an integer ratio. In all of the works reviewed so far, the focus was on the speed, while the power consumption and area usage of the CSKAs were not considered. Even for the speed, the delay of skip logics, which are based on multiplexers and form a large part of the adder critical path delay, has not been reduced.

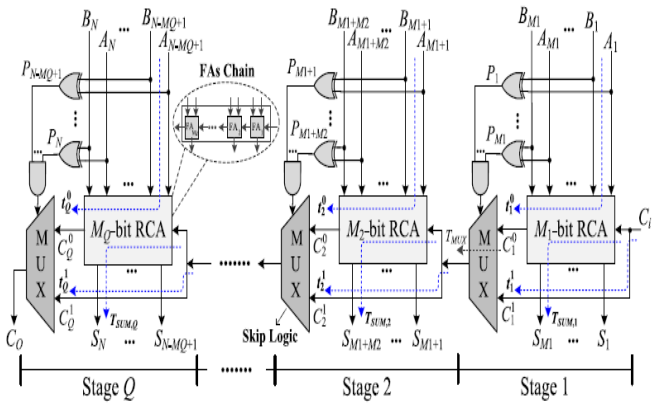

FIG. 1 Conventional Structure of the Cska

B.IMPROVING EFFICIENCY OF ADDERS AT LOW SUPPLY VOLTAGES:

To improve the performance of the adder structures at low supply voltage levels, some methods have been proposed. In adaptive clock stretching operation has been suggested. The method is based on the observation that the critical paths in adder units are rarely activated. Therefore, the slack time between the critical paths and the off-critical paths may be used to reduce the supply voltage. Notice that the voltage reduction must not increase the delays of the noncritical timing paths to become larger than the period of the clock allowing us to keep the original clock frequency at a reduced supply voltage level.

When the critical timing paths in the adder are activated, the structure uses two clock cycles to complete the operation. This way the power consumption reduces considerably at the cost of rather small throughput degradation.

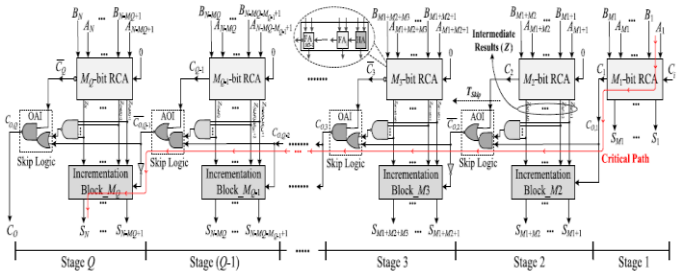

FIG 2. Existed Ci-Cska Structure

In the efficiency of this method for reducing the power consumption of the RCA structure has been demonstrated. The CSLA structure was enhanced to use adaptive clock stretching operation where the enhanced structure was called cascade CSLA (C2SLA). Compared with the common CSLA structure, C2SLA uses more and different sizes of RCA blocks.

IV. PROPOSED SYSTEM

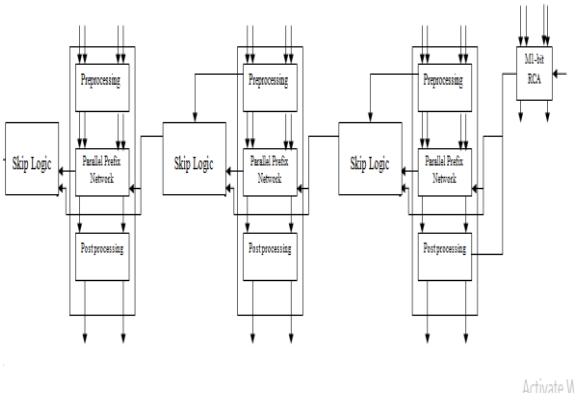

FIG 3. Structure of the Proposed Hybrid Variable Latency Cska

In the proposed hybrid structure, the prefix network of the Brent–Kung adder is used for constructing the nucleus stage. One the advantages of the this adder compared with other prefix adders is that in this structure, using forward paths, the longest carry is calculated sooner compared with the intermediate carries, which are computed by backward paths. In addition, the fan-out of adder is less than other parallel adders, while the length of its wiring is smaller. Finally, it has a simple and regular layout. The internal structure of the stage *p*, including the modified PPA and skip logic, is shown in Fig. 4. Note that, for this figure, the size of the PPA is assumed to be 8 (i.e., $Mp = 8$).

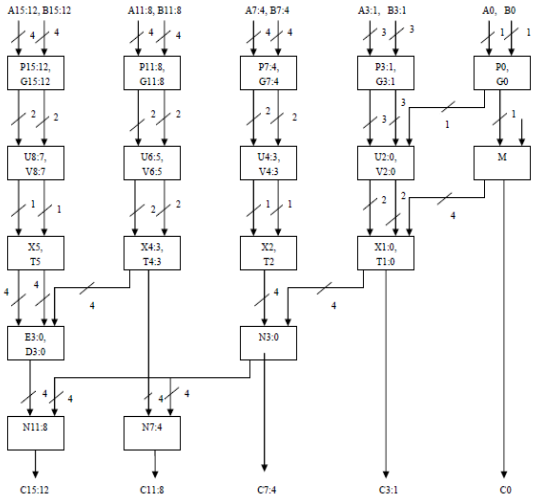

FIG. 4. 16-Bit Modified Ladner Fischer Adder

In addition, the fan-out of adder is less than other parallel adders, while the length of its wiring is smaller. The internal structure of the incrementation block, which contains a chain of half-adders (HAs), is shown in figure 4. The reason for using both NAND-NOR-Invert (NNI) and NOR-NAND-Invert (NNI) compound gates as the skip logics is the inverting functions of these gates in standard cell libraries.

V. RESULTS

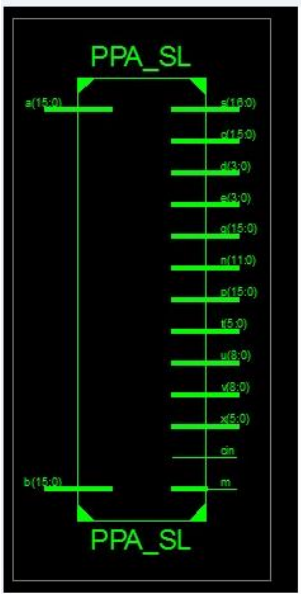

FIG 5 RTL Schematic

FIG 6. Technology Schematic

FIG 7 Output Waveform

VI. CONCLUSION

Prefix adders have been one of the most notable among several designs proposed in the past. The advantage of utilizing the flexibility in implementing the three structures based upon throughput requirements. PPA fastest adder with focus on design time and is the choice for high performance adder in industry. In this paper design and implementation of Hybrid variable latency CSKA is presented. The design shows 11.53 percentage improvement in area and 38 percentage improvement in speed when compared to CLA adder. The power consumption for Hybrid CSKA is 0.014W. The result shown that the proposed adder, parallel refix adder is faster and requires less area then carry look ahead adder.

VII. REFERENCES

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