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# A High Performance of Low Power Primary Synchronization Signal Detection in LTE

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## ABSTRACT

This paper aims to maximize through put by minimizing power. One of the approaches to attain power reduction of MIMO OFDM system by optimizing FFT architecture which is addressed in this paper. Memory has crucial importance in MIMO OFDM transceivers which are costly due to their long delay and high power consumption. An important challenging task in LTE baseband receiver design is synchronization. Conventional algorithms are based on correlation methods that involve a large number of multiplications which leads to high receiver hardware complexity and power consumption. In this brief, a hardware-efficient synchronization algorithm for frame timing based clustering and a centrally symmetric synchronization signal, this offers low matched filter implementation complexity. This presents a new synchronization method for low power and low cost design. The approach of a 1-bit analog-to-digital converter (ADC) with down-sampling is compared with that of a 10-bit ADC without down-sampling under multi-path fading conditions defined in LTE standard for user equipment (UE) performance test. The algorithm reduces the complexity of the Primary synchronization signal for LTE. Structural realization and analysis pertaining to timing, power for high performance to detect PSS detection is derived.

**Keywords:** OFDM, primary synchronization signal, correlation operation. Low power, low cost, primary synchronization signal (PSS)

## I. INTRODUCTION

The third generation Partnership project (3GPP) long term Evolution (LTE) usual is situated on orthogonal frequency division multiple-entry (OFDMA). In times when cell contraptions are getting extra widespread the cellular network are becoming more and more evolved too. Long Term evolution (LTE) in 3GPP is the present day technology in cell network that is being standardized. It's regarded as a three.9G mobile process. The title LTE comes from the advanced common terrestrial radio access community [E-UTRAN]. It's established on all web protocol organization work that isn't constrained by means of prior design. Upon call initiation, a search process carried out by way of the person apparatus (UE) is prompted to synchronize its receiver to the transmitting base station. The long term evolution (LTE) of 3GPP typical, which includes an OFDM situated downlink interface. Two synchronization channels (SCHs) were outlined the primary SCH (P-SCH) and the secondary SCH (S-SCH). For the period of synchronization, the UE receiver acquires the frame starting function, symbol timing, service frequency offset, and phone identity. While frame synchronization targets at detecting the beginning of each frame, it isn't restrained to the preliminary name setup. The UE has to periodically seek for neighboring cells for viable handovers. A Multiple input multiple output (MIMO) procedure contains more than one antenna on the transmitter and receiver ends to beef up hyperlink reliability and information premiums of the wireless verbal exchange method. Orthogonal frequency division multiplexing is effective in synchronizing the obtained sign below fading atmosphere and has been used during the past in purposes that require a huge data fee. A dedicated synchronization channel (SCH) is exact in LTE for transmitting two synchronization indicators, the primary (P-SCH) and the secondary (S-SCH). Within the SCH, each synchronization sequences are mapped on 62 subcarriers located symmetrically around the DC-provider. They are transmitted within the final two OFDM symbols of the first and sixth sub-frame (sub-frame index 0 and 5), i.e. Each 5ms. The P-SCH sign includes three size-62 Zad off-Chu sequences in frequency area which are orthogonal to each other. Each sequence corresponds to a sector identity Ns = zero,1or 2 inside a gaggle of three sectors (physical cell). If there was once only one cell-common P-SCH,UE's at the cell edge would experience a composite channel from a couple of cells, which would effect in channel estimates that don't reflect the individual channels to the respective cells. Therefore, 3 unique P-SCH signals are outlined, more often than not to be assigned in order that neighbor cells use special P-SCH indicators. To obtain symbol synchronization, the UE as a result has to correlate with the 3 P-SCH indicators in parallel, to assess the correct P-SCH sign and the right timing thereof.

LTE uses orthogonal frequency division multiple access in the uplink. It has evolved EDGE capabilities available to significantly increases EDGE throughput rates and announced deployment. LTE introduced for next generation throughput performance using 2x2 MIMO. Advanced core architecture available through EPC primary for LTE. Providing benefits such as integration of multiple network types and flatter architecture for better latency performance. LTE enhancement such as 4x MIMO and dual carrier available.

**The primary synchronization signal in E-UTRA**

In E-UTRA, the bandwidth is divided into useful resource blocks of 180 kHz width. A few bandwidths (as much as 20 MHz) are supported and the minimum system bandwidth (1.25 MHz) corresponds to 6 resource blocks. With 15 kHz subcarrier spacing, the synchronization sign may just occupy at most 72 subcarriers, which would ordinarily be generated by way of an N=128 factor FFT. None the less, to permit matched filter implementations with lengths shorter than 128 samples, the P-SCH signals are defined as OFDM alerts with up to sixty four subcarriers, including DC subcarrier. Such a sign can be detected by using a matched filter of size 64.

$$d_u(n) = \begin{cases} e^{-j\frac{\pi u n(n+1)}{63}} & n = 0,1,\ldots,30 \\ e^{-j\frac{\pi u(n+1)(n+2)}{63}} & n = 31,32,\ldots,61 \end{cases} \quad (1)$$

The synchronization sign design emanated in a frequency area outlined ZC sequence of length sixty three, with the core detail punctured. Thus 62 energetic subcarriers are used, situated on the DC subcarrier. The sequence is given by

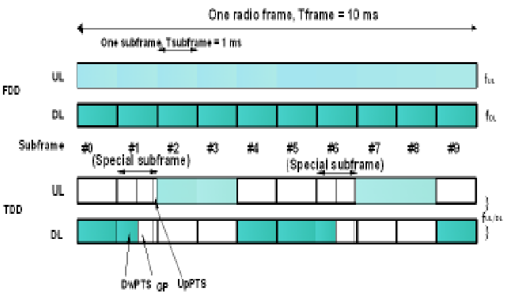


**Figure 1.** PSS detection Frame structure

The foremost function of PSS is to observe the boundary of a frame the place non-coherent detection system needs to be used at the receiver in view that there's no recognized reference understanding originally. Matched filter is a common non-coherent detection procedure that can be used to observe PSS efficaciously. The sequence in is mapped to the subcarriers around DC and changed to time area by using 64-factor IDFT. To realize this signal at the receiver, the correlation with the time domain sign of the ZC sequence is calculated in (2).

$$C_u(m) = (W^H d_u)^H y \qquad (2)$$

Where y is the successive 64-by-1 received signal vector, W is the DFT matrix, and $d_u$ is 64-by-1 vector composed of $d_u(m)$ is punctured at DC.

Then, from (2), the coefficients of the matched filter can be obtained in (3)

$$coeff = (W^H d_u)^H \qquad (3)$$

Where

$$coeff = [coeff(63)coeff(62)..coeff(1)coeff(0)]$$

and the matched filter can be expressed

$$MF = \sum_{k=0}^{63} coeff\,(k)y(t-k) \qquad (4)$$

Where $y(k)$ is the received signal.

## II. BACKGROUND

As of the power consumption perception, more power is dropped for a 10-bit analog-to digital conversion than a 1-bitADC, as 10-bit pipelined ADC has several power amplifiers in it. To move toward low-power resolution, a method of PSS detection using 1-bit ADC is proposed. The transfer of PSS is done twice for every 10ns. The sampling rate of the receiver is 122.88 MHz; however, the date rate of input data to the matched filter is 1.92 MHz. Thus, 9600 samples need to be buffered by the matched filter as output for every 5ms, which is not area and cost efficient. To come up with a low cost solution, a method of down-sampling by 8 is used at the output of matched filter. Primary synchronous signal is designed for cell search and handover in 3GPP LTE systems, which is transmitted every 5 ms. Search time of PSS detection is an important criterion when measuring its performance. As discussed before about Multi input and Multi output in LTE, We assume that there are four receive antennas and four transmit antennas in the simulated LTE MIMO system.

### A. Hardware implementation of matched filter and PSS detector with one memory

Matched filter plays a relevant role in PSS detection. The matched filter is a predominant element within the PSS detection. A 64 tapped matched filter proven if determine (4) is used, which calculate 64 difficult multiplications. When you consider that 84 matched filters are required within the process, a complete of 5376 models of elaborate multiplication is needed, which is high fee and low efficient in receiver side. The practical implementation of this matched filter can also be problematic. Excessive power consumption may lead to inaccurate outcome which results at receiver not to detect correct signal. As of having non-coherent nature of matched filter if it influences it results in much less affectivity of main synchronous detection.

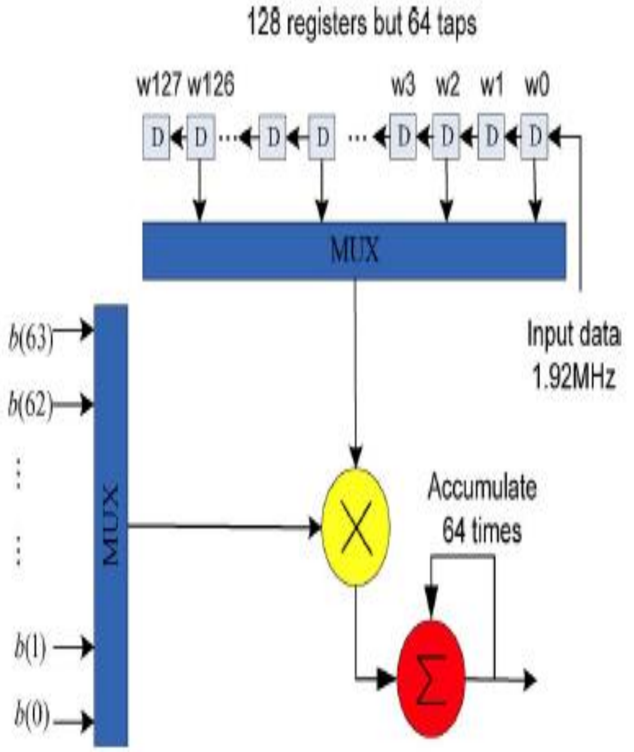

**Figure 2.** Matched filter.

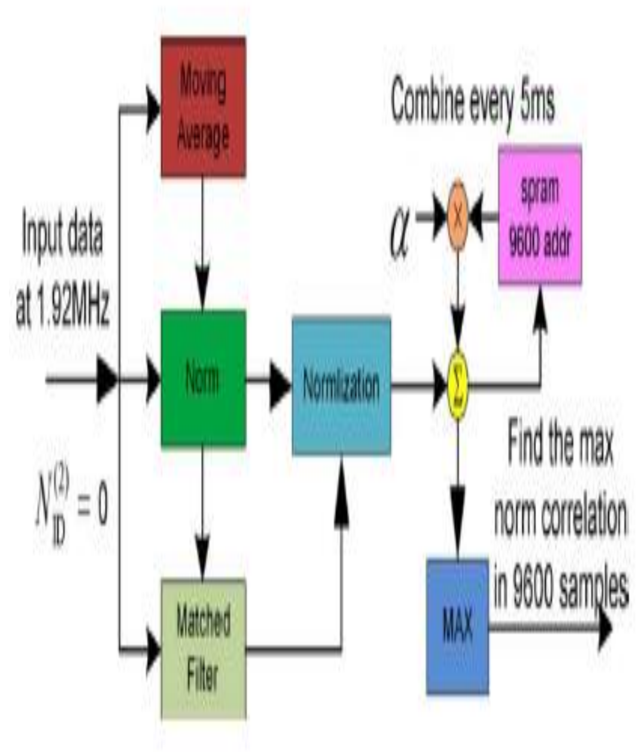


**Figure 3.** PSS detection architecture.

The above figure clearly briefs the PSS architecture for detection which includes a single ram memory. This architecture is without down sampling. Where 9600 samples are to be store, which makes more area to consume.

## III. PROPOSED SYSTEM

For the reason that 84 matched filters are required within the system, a total of 5376 units of difficult multiplication is needed, which is not cheap for a sensible communication as a result of high price of multiplication unit in the receiver. In practice, the sampling expense of input data to the matched filter is 1.92 MHz while the method clock is 122.88 MHz, which means that we can use only one complicated multiplication throughout 64 cycles instead of making use of sixty four units of difficult multiplication shown in fig.2. For that reason, 84 models of elaborate multiplication are adequate for the whole process. Therefore, best 1200correlation values have to be stored in RAM with 1200 addresses, which scale back the RAM dimension of the entire approach with the sample of a component of nearly 8. This architecture is much smaller than that of the orthogonal structure is much smaller than that of the normal architecture, which reduces the cost of the chip significantly. From the power viewpoint, not only 10-bit ADC reduces the power consumption, but the hardware of digital good judgment additionally does.

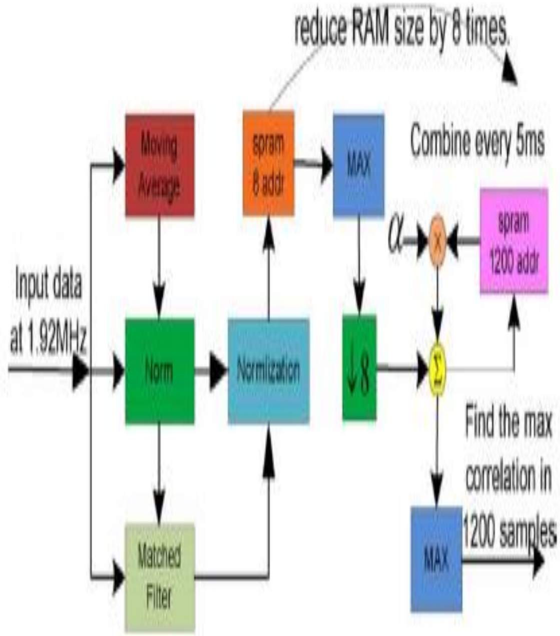


**Figure 4.** Area efficient PSS detection architecture

### Modified area efficient architecture

The area efficient architecture is modified by changing matched filter design and making the PSS samples in to cluster to attain less complex multiplications. As a result delay of modified circuit reduces which gives high performance.

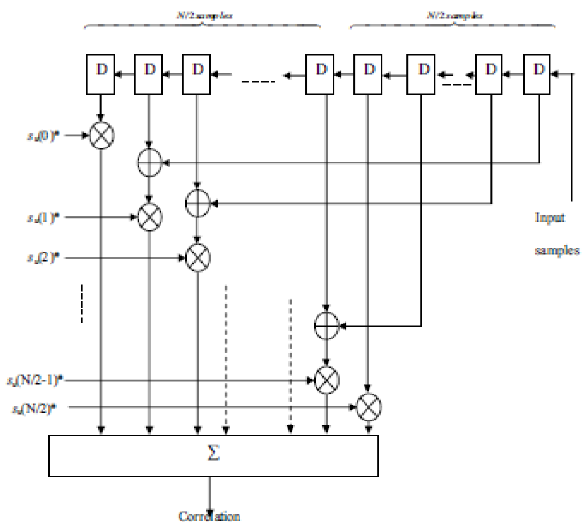


**Figure 5.** Centrally symmetric matched filter

The above matched filter center symmetric one. The central symmetry of *N*-1 samples of a P-SCH signal can be used to reduce the number of multiplications in the corresponding matched filter. For example, if *N*=64, there are 62 centrally symmetric samples of the P-SCH signal. These sample pairs can be added prior to multiplication, so the matched filter can be implemented by reduced multiplications per single correlation. The complex multiplication can also be reduced by clustering the PSS samples, means grouping the similar samples for addition and then go for multiplication.

## IV. APPROXIMATE RESULTS AND DISCUSSION

The comparison of normal architecture of PSS detection with area efficient architecture, which included centrally symmetric matched filter in terms of area, power, delay are shown in the following table 1.

**Table 1.** Comparison of architectures

| Architecture | Area | Power | Delay |
|---|---|---|---|
| Normal architecture | 6343 | 2.646 | 5.212 |
| Modified area efficient architecture | 3437 | 1.104 | 4.582 |

**Block diagram:**

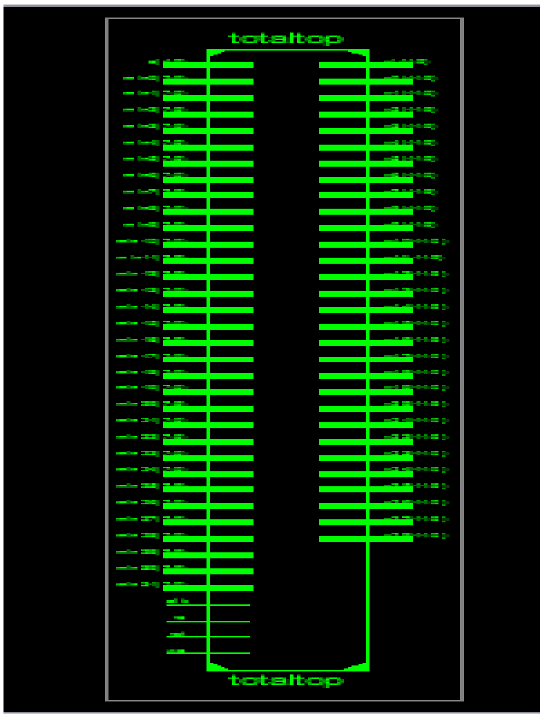


**Figure 6**

**RTL schematic:**

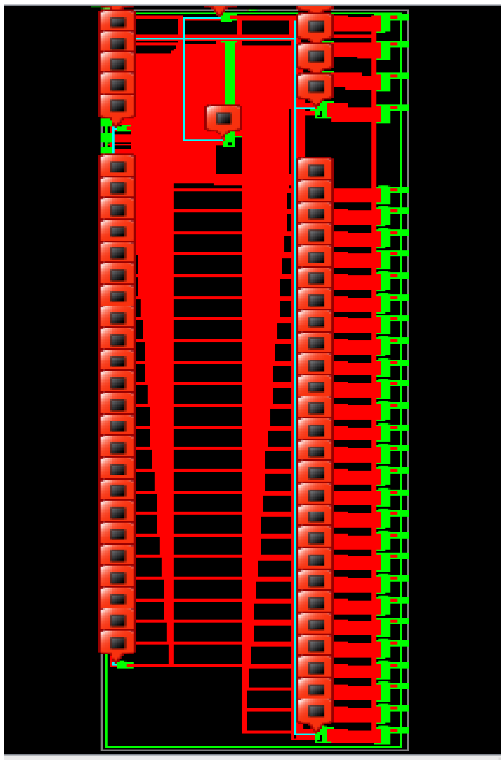

**Figure 7**

**Simulation results:**

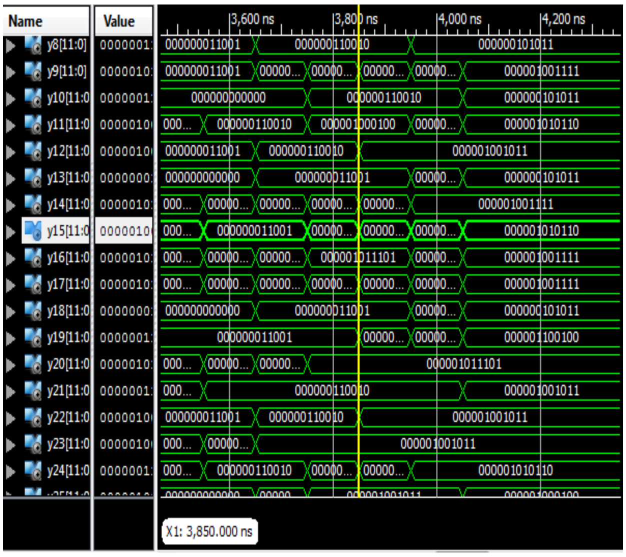


**Figure 8**

## V. CONCLUSION

This paper presents VLSI implementation of PSS detection in LTE with excessive throughput MIMO OFDM transceiver. As the discipline and energy consumption of the normal implementation structure are too significant acceptable, and to put into effect, so a more functional implementation structure is proposed where PSS is detected effectively and safely. A centrally symmetric synchronization sign, which offers low matched filter implementation complexity, has been offered. The important symmetry allows for including symmetric samples prior to multiplication, thereby reducing the multiplication effort through 1/2. For that reason a a lot minimize power and low cost which renders its viable within the implementation of UE chip.

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