Design and Implementation of Carry Look Ahead Adder In Qunatum Dot Cellular Automata

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ABSTRACT

In nano scale logic computing, dissipated heat and device area are the key areas of interest. Ideally zero heat dissipation can be achieved in reversible circuits by preserving information. This paper presents an original method and a practical design implementation of carry look ahead Adder.Among several nano-devices, QCA has elevated functionality in designing circuits at nano scale. A circuit for carry look ahead generator and its realization in QCA has been reported in this paper. To achieve the proposed design, majority gate based AND operation and OR operations have been used to design an EX-OR.These designs are verified and compared with a ripple carry adder. This comparison establishes the computing accuracy of the proposed designs. The design can function as a heart for faster parallel adder at nano scale level.

Keywords : Quantum dot Cellular Automata (QCA), Ripple Carry adder, Carry look ahead Adder

I.   INTRODUCTION

CMOS Technology:

Microprocessor manufacturing processes was governed by Moore's law, and consequently microprocessor performance till now. Today many integrated circuits are manufactured at 0.25-0.33 micron processes. But recent studies indicate that as early as 2010, the physical limits of transistor sizing may be reached however the performance of various circuits in current CMOS-based architectures is close to reaching the limit. If the feature size of transistors is further reduced to a nanometer, it will produce quantum effects such as tunneling. Further, during device scaling process due to the effects of wire resistance and capacitance, the interconnections never scale automatically.

An Introduction to QCA Technology As an alternative to CMOS-VLSI, an approach called the quantum cellular automata (QCA) is developed in 1993 to computing with quantum dots. Unlike conventional computers in which information is transferred from one place to another by electrical current, QCA transfers information by means of propagating a polarization state from one cell to another cell. Hence improving the speed by reduction in area is the main area of research in VLSI system design.

In QCA device, the binary data is stored through charge on electrons located within QCA dots rather as electrical power like in conventional CMOS system QCA cells are interacted by columbic interaction caused propagation of information into QCA wires. This paper shows the circuit design for carry look ahead Adderand its implementation in QCA. The designs are simulated on QCA Designer-2.0.3 simulator.

The rest of this paper is framed as follows. Section II presents the review of earlier work, Section III presents about Quantum Dot Cellular Automata,

Section IV presents about proposed Reversible Carry look ahead adder. Section V describes the simulation information of proposed Carry Look Ahead adder and finally Section VI concludes the paper.

II. REVIEW OF EARLIER WORK

Arithmetic operations like addition, subtraction, multiplication, division are basic operations to be implemented in digital computers using basic gates like AND, OR, NOR, NAND etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication (by repeated addition), subtraction (by negating one operand) or division (repeated subtraction).

It is possible to create a logical circuit using multiple full adders to add N-bit binary numbers. Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is a RippleCarryAdder, since each carry bit "ripples" to the next full adder. The first full adder may be replaced by a half adder if there is no carry input.

2.1 One-bit full adder:

A one-bit full adder is a combinational circuit that forms the arithmetic sum of three bits. It consists of three inputs(A, B and Cin) and two outputs (S and Cout) as illustrated in Figure below
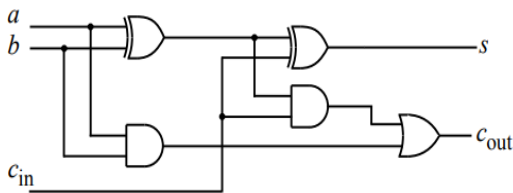

Figure 1. A 1bit Full adder

Inputs			Outputs	
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1. Functional table of 1 bit Full adder

2.2 4bit Ripple carry adder:

Figure 2 shows the interconnection of four full adder (FA) circuits to provide a 4-bit ripple carry adder. Notice from Figure 2 that the input is from the right side because the first cell traditionally represents the least significant bit (LSB). Bits a_0 and b_0 in the figure represent the least significant bits of the numbers to be added. The sum output is represented by the bits $S_3 to S_0$ and carry output is C_4
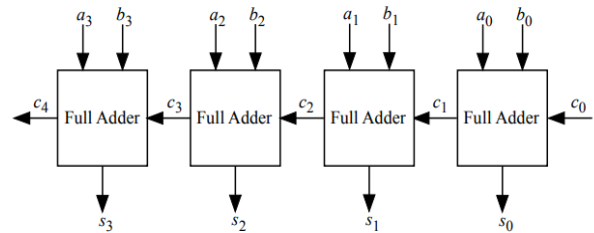

Figure 2. 4-Bit ripple carry adder

In the ripple carry adder, the output is known after the carry generated by the previous stage is produced. Thus, the sum of the most significant bit is only available after the carry signal has rippled through the adder from the least significant stage to the most significant stage. As a result, the final sum and carry bits will be valid after a considerable delay. To overcome the drawback of this Ripple carry adder we propose a Carry look ahead adder where the carry rippling is no there and the internal carries are generated in before So that the propagation time will be less.

III. QUANTUM DOT CELLULAR AUTOMATA

Quantum-dot cellular automata is a computing paradigm using arrays of nanostructures called

quantum dots Quantum dots are nanostructures created from standard semi conductive materials such as *Si/SiO2*. These structures can be modeled as 3-dimensional quantum wells. As a result, they exhibit energy quantization effects even at distances several hundred times larger than a material's lattice constant.

Quantum cellular automata (QCA) is a new technology in nano meter scale (<18nm) to support nanotechnology. QCA is very effective in terms of high space density and power dissipation and will be playing a major role in the development of the Quantum computer with low power consumption and high speed. And a Quantum Dot cellular Automata (QCA) is an emerging technology that takes advantage of quantum effects, which become increasingly apparent at the scale of a few nanometers.

The QCA cell [9] consists of a system of four quantum dots charged with only two free electrons. Electrostatic repulsion between these electrons forces them to occupy only the diagonal sites creating a so called "polarization" used to encode binary information.

In QCA all the Logic Operations are must be generated with Majority Logic Gate only. The structure of majority gate is given below

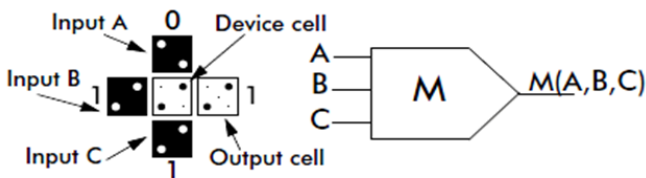$$M(A, B, C) = AB + BC + AC$$

Figure 3. Majority gate in QCA

If we Fixed polarize any one input of a majority gate to 0 then that majority gate will be act as AND gate. If we Fixed polarize any one input of a majority gate to 1 then that majority gate will be act as OR gate.

Inputs			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

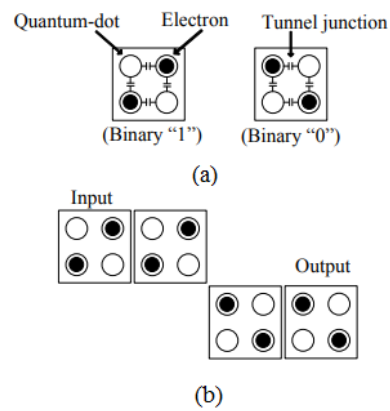Table 2. Functional Table of QCA Majority Gate

Figure 3 (a). QCA Cell with polarization 1 and 0 (b) QCA Inverter structure

QCA CLOCKING

The clocking of QCA is accomplished by controlling the potential barriers between adjacent quantum-dots. When tunneling potential is high the electron wave functions become de-localized causing indefinite polarization. Raising the potential barrier decreases the tunneling potential, as a result the electrons begin to localize. Once the electrons localize the cell gains a definite polarization.
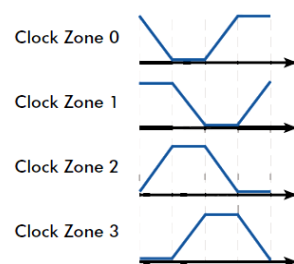

Figure 4. QCA clock zones

IV. PROPOSED CARRY LOOK AHEAD ADDER

Carry propagation time is a limiting factor on the speed with which two numbers are added in parallel. Since all other arithmetic operations are implemented by successive additions, the time consumed during the addition process is very critical. An obvious solution for reducing the carry propagation delay time is to employ faster gates with reduced delays. The most widely used technique called carry look-ahead.

The carry look ahead adder (CLA) has a regular structure. It achieves high speed. In this paper we design a 4 bit CLA. This design employs 4 bit slices for the look ahead logic By the nature of QCA cells the carry look ahead adder is pipelined. In the PG block we have a generated output that indicates that a carry is "generated "at bit position and a propagate output that indicates that a carry entering bit position will propagate to the next bit position. Thus these are used to produce all the carries in parallel at the successive blocks. Due to the pipeline diagram all sum signals are available at the same clock period. The carry propagate and carry generate bits are calculated based on those bits we can calculate the intermediate carries with the help of carry input

$$P_i = A_i \oplus B_i$$
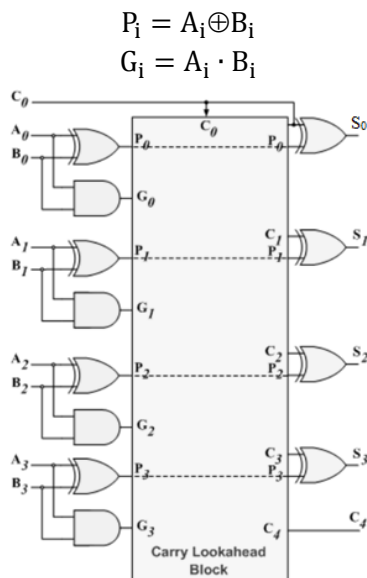$$G_i = A_i \cdot B_i$$

Figure 5. 4bit Carry Look Ahead Adder

The outputs of sum and carry can be defined as
$$S_i = P_i \oplus C_i$$
$$C_{i+1} = G_i + P_i C_i$$

The 4-bit carry look-ahead (CLA) adder consists of 3 levels of logic:

First level: Generates all the P & G signals. Four sets of P & G logic (each consists of an XOR gate and an AND gate).

Second level: The Carry Look-Ahead (CLA) logic block which consists of four 2-level implementation logic circuits. It generates the carry signals (C1, C2, C3, and C4) as defined by the above expressions

Third level: Four XOR gates which generate the sum signals (Si) ($Si = Pi \oplus Ci$).

V. SIMULATION RESULTS

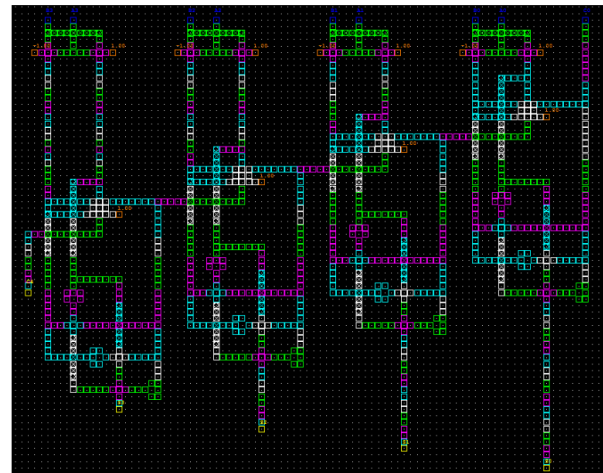*4-bit Ripple Carry Adder:*

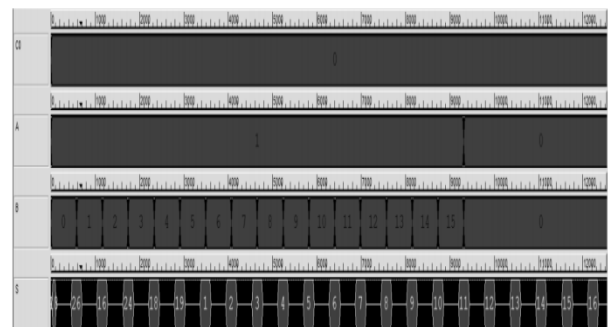Figure 6. Layout design of 4-bit Ripple carry adder

Figure 7. Simulated Output of a 4-bit Ripple carry adder
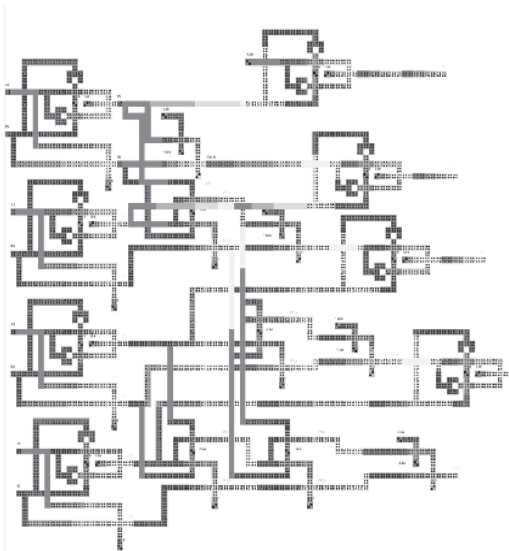
4-Bit Carry Look Ahead Adder

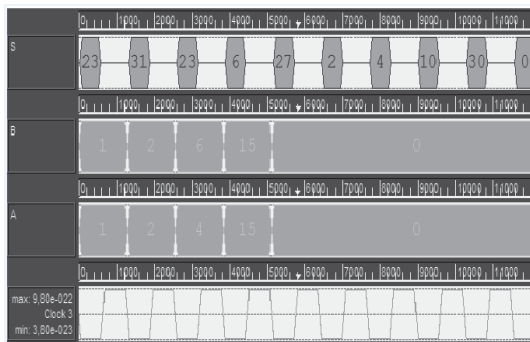Figure 8. Layout design of 4-bit Carry look ahead
adder

Figure 9. Simulation Output of A 4-Bit Carry look
ahead adder

VI. CONCLUSION

In this paper we propose a new carry look ahead adder which gives better result in terms of delay compared to ripple carry adder. The propagation delay is less in the proposed CLA where it is high in ripple carry adder. And are designed and simulated in QCA Designer 2.3.0 tool

VII. REFERENCES

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