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Design of Weighted Pseudorandom Test Pattern Generation for BIST Implementation Using Low Power

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ABSTRACT

This paper presents, the generation of significant power droop (PD) during at-speed test performed by Logic Built-In Self Test (LBIST) is a serious concern for modern ICs. In fact, the PD originated during test may delay signal transitions of the circuit under test (CUT): an effect that may be erroneously recognized as delay faults, with consequent erroneous generation of test fails and increase in yield loss A new low-power (LP) scan-based built-in self test (BIST) technique is proposed based on weighted pseudorandom test pattern generation and reseeding along with. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST. During at-speed test of high performance sequential ICs using scan-based Logic BIST, the IC activity factor (AF) induced by the applied test vectors is significantly higher than that experienced during its infield operation. Consequently, power droop (PD) may take place during both shift and capture phases, which will slow down the circuit under test (CUT) signal transitions. At capture, this phenomenon is likely to be erroneously recognized as due to delay faults. As a result, a false test fail may be generated, with consequent increase in yield loss. In this paper, along with pseudorandom testing and deterministic BIST proposes another approaches to reduce the PD generated at capture during at-speed test of circuits with scan-based Logic .During the pseudorandom testing Phase, by disabling a part of scan chains an LP weighted random test pattern generation scheme is achieved. During the deterministic BIST phase, the design-for-testability architecture by slight modification of LFSR and fault coverage is increases and power is reduced by this approaches.

Keywords: Built in Self-Test, LFSR, Low power, Circuit under test.

I. INTRODUCTION

The continuous scaling of microelectronic technology enables to keep on increasing ICs' integration density and performance. This comes together with new challenges for system test and reliability. In particular, during at-speed test of high performance circuit using scan (for instance microprocessors), the IC activity factor (AF) induced by the applied test vectors is significantly higher than that experienced during its infield operation. Consequently, power droop (PD) may take place during both shift and capture phases, which will slow down the circuit under test (CUT) signal transitions. At capture, this phenomenon is likely to be erroneously recognized as due to delay faults. As a result, a false test fail may be generated, with consequent in-crease in yield loss. The aggressive scaling of microelectronic technology is enabling the fabrication of increasingly complex ICs. Together with several benefits (improved performance, decreased cost per function, etc.), this poses serious challenges in terms of test and reliability. In particular, during at-speed test of high-performance microprocessors, the IC activity factor

(AF) induced by the applied test vectors is significantly higher than that experienced during in field operation. Consequently, excessive power droop (PD) may be generated, which will slow down the circuit under test (CUT) signal transitions. This phenomenon is likely to be erroneously recognized as due to delay faults. As a result, a false test fail will be generated, with consequent increase in yield loss.

Recent methods aim at reducing the switching activity during scan shift cycles, whose test generator allows automatic selection of their parameters for LP pseudorandom test generation. However, many of the previous LP BIST approaches cause fault coverage loss to some extent. Therefore, achieving high fault coverage in an LP BIST scheme is also very important. Weighted pseudorandom testing schemes and methods, can effectively improve fault coverage. However, these approaches usually result in much more power consumption due to more frequent transitions at the scan flip flops in many cases. Therefore, we intend to propose an LP scan-based pseudorandom pattern generator (PRPG). This is one of the major motivations of this paper. Most of the previous deterministic BIST approaches did not include LP concerns. We intend to present a new method that effectively combines an efficient LP PRPG and LP deterministic BIST. In order to reduce test power in deterministic BIST, we will propose a new LP reseeding scheme, since there is no other effective solution in this field. This is another motivation of this paper. Some approaches have been proposed in the literature to reduce the PD for combinational LBIST, while fewer approaches exist for scan-based LBIST. The solutions for combinational LBIST modify the internal structure of traditional LFSRs to generate intermediate test vectors. Such vectors are inserted between each couple of original test vectors, and enable to reduce the AF of the CUT inputs, thus also the whole CUT AF. Therefore, PD is reduced as well. However, these techniques are not effective in reducing PD at capture in scan-based LBIST. To reduce PD at capture in scan-based LBIST, the solutions have been proposed. Particularly, PD is reduced by alternately disabling groups of scan chains during test. This is a successful approach to reduce PD at capture during scan-based LBIST, for both the LOC and the LOS schemes. However, it requires a significant increase in number of test vectors, and consequently test time, to achieve the same Fault Coverage (FC) as with conventional scan-based LBIST. In this paper, we propose a new LP scan-based BIST architecture, which supports LP pseudorandom testing, LP deterministic BIST and LP reseeding.

II. RELATED WORK

We consider the conventional scan-based LBIST (Conv-LBIST) architecture shown in Fig. 1. The state flip-flops (FFs) of the CUT are scan FFs, arranged into many scan chains (s scan chains in Fig. 1).The pseudorandom pattern generator is implemented by an LFSR. The PS, which reduces the correlation among the test vectors applied to adjacent scan-chains, is composed of an XOR network expanding the number of outputs of the LFSR to match the number of scan chains s . Scan flip flops, especially, the ones close to the scan-in pins, are not observable in most of shift cycles. proposed a novel BIST scheme that inserts multiple capture cycles after scan shift cycles during a test cycle. Thus, the fault coverage of the scan-based BIST can be greatly improved. An improved method of the earlier work, presented, selects different numbers of capture cycles after the shift cycles. In this paper, a new LP scan-based BIST technique is proposed based on weighted pseudorandom test pattern generation and reseeding. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST. New pseudorandom test generators were proposed to reduce power consumption during testing. A new encoding scheme

is proposed in, which can be used in conjunction with any LFSR-reseeding scheme to significantly reduce test power and even further reduce test data volume. Lai *et al.* proposed a new LP PRPG for scan-based BIST using a restricted scan chain reordering method to recover the fault coverage loss. A low-transition test pattern generator in was proposed to reduce the average and peak power of a circuit during test by reducing the transitions among patterns. A new adaptive low shift power pseudorandom test pattern generator was presented to improve the tradeoff between test coverage loss and shift power reduction in logic BIST. This is achieved by applying the information derived from test responses to dynamically adjust the correlation among adjacent test stimulus bits. It is possible to implement LP scan testing in a test compression environment without any increase on test application cost .A new scan architecture to compress test data and compact test responses for delay testing. An important TSV modeling/simulation technique.

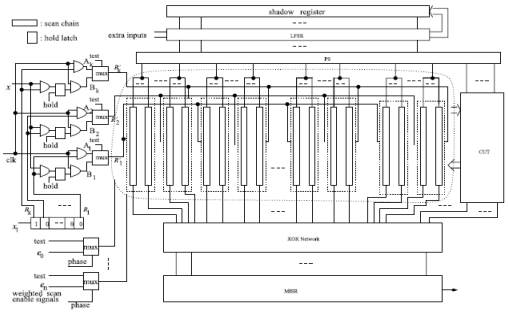

Figure 1. General DFT architecture for LP scan-based BIST.

III. CONSIDERED SCENARIO

Weighted Pseudorandom Test Pattern Generation Our method generates the degraded sub circuits for all subsets of scan chains in the following way. All PPIs related to the disabled scan chains are randomly assigned specified values (1 and 0). Note that all scan flip flops at the same level of the same scan tree share the same PPI. For any gate, the gate is removed if its output is specified; the input can be removed from a NAND, NOR, AND, and OR gates if the input is assigned a non controlling value and it has at least three inputs. For a two-input AND or OR gate, the gate is removed if one of its inputs is assigned a non controlling value. For a NOR or NAND gate, the gate degrades to an inverter if one of its inputs is assigned a non controlling value. For an XOR or NXOR gate with more than three inputs, the input is simply removed from the circuit if one of its inputs is assigned value 0; the input is removed if it is assigned value 1, an XOR gate changes to an NXOR gate, and an NXOR gate changes to an XOR gate. For an XOR gate with two inputs, and one of its inputs is assigned value 0, the gate is deleted from the circuit. For a two-input NXOR gate, the gate degrades to an inverter. If one of its inputs is assigned value 1, a two-input XOR gate degrades to an inverter. If one of its inputs is assigned value 1, a two-input NXOR gate can be removed from the circuit. We first propose a new procedure to generate the weights of the test-enable signals for all scan chains in the LP DFT circuit after the degraded sub circuits for each subset of scan chains, which are driven by a single clock signal, have been produced. The i -controllability $C\_i(l)$ ($i \in \{0, 1\}$) of a node l is defined as the probability that a randomly selected input vector sets l to the value i . The observability $O\_(l)$ is defined as the probability that a randomly selected input vector propagates the value of l to a primary output.

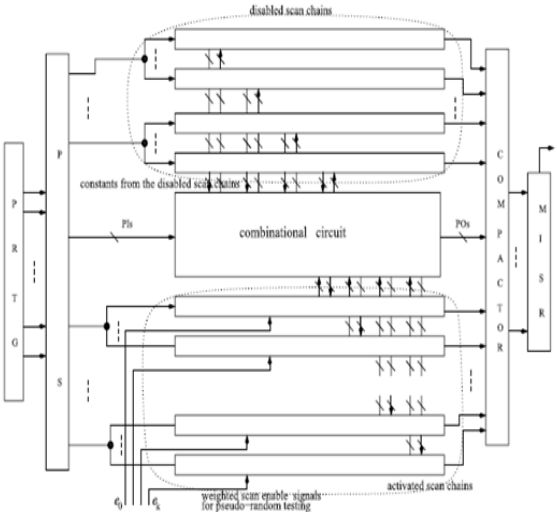

Figure 2. Weighted pseudorandom test generator for scan-tree-based LP BIST

The signal probability of a node is defined in the same manner as its 1-controllability measure. In the scan-based BIST architecture, as shown in Fig. 1, different weights e0, e1, . . ., and ek are assigned to the test enable signals of the scan chains SC0, SC1, . . ., and SCk , respectively, where e0, e2, . . . , ek ∈ {0.5, 0.625, 0.75, 0.875}. Scan flip flops in all disabled scan chains are set to constant values. Our method randomly assigns constant values to all scan flip flops in the disabled scan chains. The circuit is degraded into a smaller sub circuit. All weights on the test enable signals are selected in the degraded sub circuit. The gating logic is presented in Fig. 1. We do not assign weights less than 0.5 to the test-enable signals, because we do not want to insert more capture cycles than scan shift cycles. We have developed an efficient method to select weights.

We use the same LFSR for both pseudorandom pattern generation and deterministic phases. First, we propose a new algorithm to select a proper primitive polynomial; after that the LP deterministic BIST and LP reseeding schemes are presented. Some extra variables are injected just like EDT .We propose a new scheme to select the size of the LFSR and the number of extra variables simultaneously in order to minimize the amount of deterministic test data. Usually, a small LFSR constructed by a primitive polynomial is sufficient when a well-designed PS is adopted in the pseudorandom testing phase. In our method, a combination of a small LFSR and the PS is used to generate test patterns in the pseudorandom testing phase. The weighted test-enable signal-based pseudorandom test generator generates weighted pseudorandom test patterns. The size of the LFSR is not determined by the maximum number of care bits for any deterministic test vector. That is, the same LFSR is used for both phases.

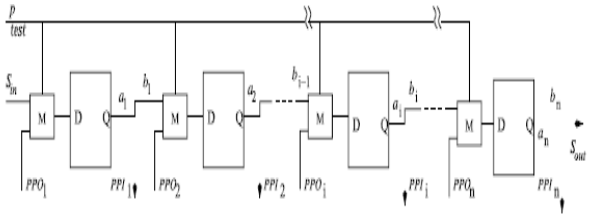

Figure 3. Scan chain with a weighted test-enable signal.

A well-designed LFSR is needed in order to encode all deterministic vectors after the pseudorandom testing phase. A new procedure is proposed to select a primitive polynomial with the minimum degree that can encode all deterministic test vectors for the hard faults. An efficient algorithm, as presented in Algorithm 2, is used to generate primitive polynomials of any desired degree. For any $i \leq 30$, assume that all primitive polynomials are kept in *Qi*. As for $i > 30$, only a number of primitive polynomials are provided in Qi. The following procedure returns a primitive polynomial with the minimum degree that encodes all deterministic vectors for the random pattern- resistant (hard) faults.

As previously introduced, the goal of our approach is to reduce the CUT AF at capture, since this is the AF that may result in the generation of a false test fail during LBIST.As stated above, such a CUT AF is proportional to the AF of the scan chains at the last (*n-th*) shift CK[6], which is equal to the number of bits in the scan chains that change logic value between the *(n-1)-th* and the *n-th* shift CKs. To reduce the CUT AF at capture, our approaches reduce the AF of all scan chains between the *n-th* shift CK and the previous *(n-1)-th* shift CK, by properly modifying *n 1*bits out of the *n* bits to be loaded in the scan chains.

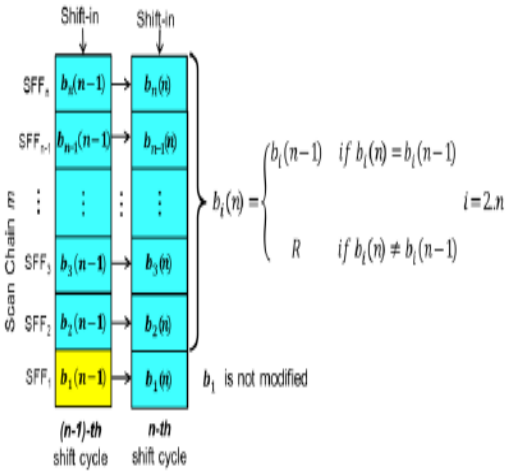

Figure 4. Schematic representation of the LCA modification of the bits to be loaded in a generic scan chain *m* (*m=1..s*).

In order to derive a mathematical description of our proposed solution, we make the following simplifying assumptions for Conv-LBIST.

1) All scan chains have the same number of scan FFs.

2) The maximum AF between two following test vectors T m i and T i+1 is the same for all scan chains (m = 1 . . . s).

IV. RESULTS

Block Diagram

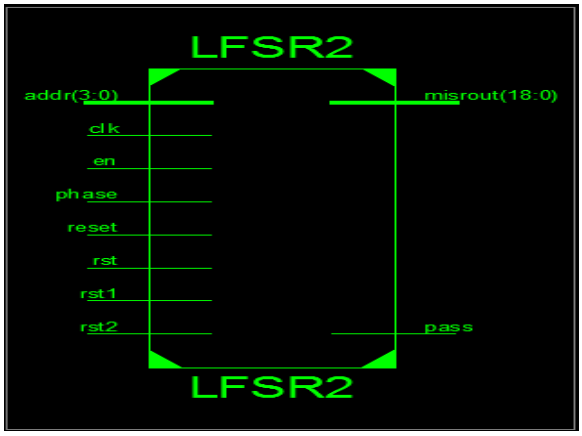

Figure 5

RTL schematic

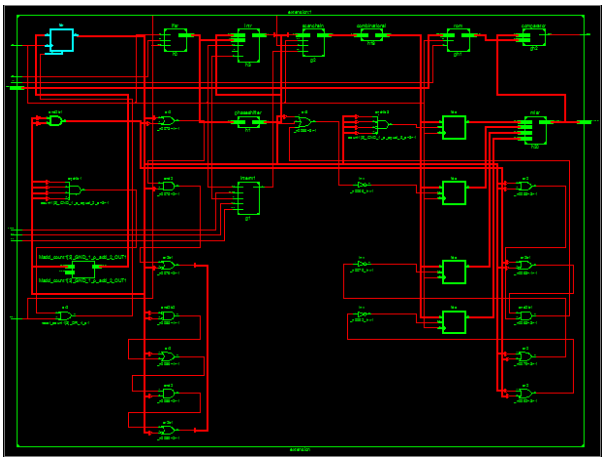

Figure 6

Technology Schematic

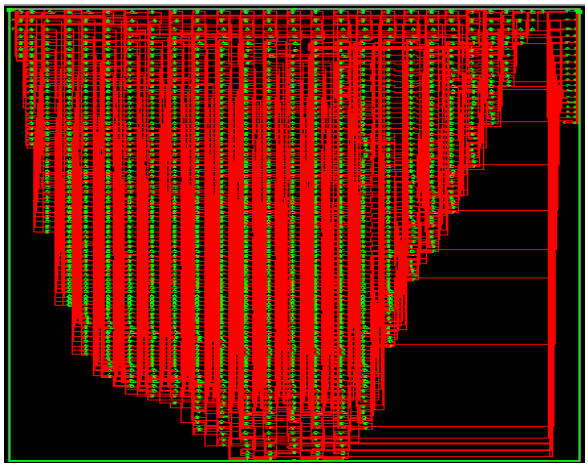

Figure 7

Simulation Results:

Figure 8

Comparison Table 1

	Existing	Proposed
Area (LUT)	31	138
Delay (ns)	1.285	1.207
Power (watts)	0.302	0.295

V. CONCLUSION

A new LP BIST method has been proposed using weighted test-enable signal-based pseudorandom test pattern generation and LP deterministic BIST and reseeding. The new method consists of two separate phases: 1) LP weighted pseudorandom pattern generation and 2) LP deterministic BIST with reseeding. The first phase selects weights for test-enable signals of the scan chains in the activated sub circuits. The proposed solution enables designers to reduce the probability that the delay induced by PD exhibited during at-speed test is erroneously interpreted as a delay fault, with consequent generation of a false test fail. This is achieved by reducing the AF of the CUT compared with conventional scan-based LBIST, by proper modification of the test vectors generated by the LFSR A new procedure has been proposed to select the primitive polynomial and the number of extra inputs injected at the LFSR. A new LP reseeding scheme, which guarantees LP operations for all clock cycles, has been proposed to further reduce test data kept on-chip. Experimental results have demonstrated the performance of the proposed method by comparison with a recent LP BIST method. The LP reseeding technique is a little more complicated. This work can be extended to latch-on-capture transition fault testing and small delay defect testing.

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