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Multiple Error Detection and Correction in SRAM Emulated TCAMs Using RS Code

Sumukh G*, Nazim Khan, Priyadarshini S, Dr. Vrunda Kusanur, Dr. Keerti Kulkarni

*Department of Electronics and Communication, BNMIT, Bengaluru, Karnataka, India

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ABSTRACT

Ternary Content Addressable Memories (TCAMs) are specialized types of memory primarily used in networking hardware, such as switches and routers, to perform high-speed operations. They are mainly utilized in hardware components designed for fast searching and matching operations. For example, TCAMs are used in intrusion detection and prevention systems (IDS/IPS) and network and packet processing in software defined system SDNs. TCAMs are used in application specific integrated circuits which are integrated into intellectual property blocks or as a standalone device. The FPGAs do not include any blocks for TCAMs. however, the flexibility of the FPGAs makes them dependable for implementation. The major issue caused while operating on TCAMs is soft errors which corrupt the stored bits. Memories can be protected using a parity bit which is an extra bit, needs an extra bit of memory or cyclic redundancy check used to verify data integrity by generating a checksum during data writing and comparing it during reading. The major drawback of using these methods is that these can only detect single bit error, to detect multiple bit errors we need error correcting codes (ECC). In this work Reed-Solomon code is used for correcting multiple bit errors.

Keywords: Ternary content addressable memories (TCAMs), Field programmable gate, soft errors arrays (FPGA), Intrusion detection and prevention systems (IDS/IPS), Error correcting codes (ECC). Reed Solomon code (RS).

Introduction

Research led by Intel [3] revealed that cosmic radiation-induced failures increase at higher altitudes, but even ground-level electronic devices are now at risk. Among the most vulnerable are SRAM-based components, which are highly sensitive to radiation. SRAM serves as a cache memory for processors, offering rapid access to frequently used data. Unlike DRAM, which demands constant refreshing, SRAM retains data without periodic recharging, allowing processors to fetch data without delays, leading to faster performance. However, SRAM's reduced supply

voltage in newer fabrication nodes lowers cell capacitance, making memory cells more prone to bit flips caused by cosmic rays or alpha particles. Additionally, the trend of increasing SRAM density to improve latency makes these chips even more susceptible to radiation exposure. Packaging materials used in semiconductor fabrication often contain trace amounts of radioactive elements, further increasing the likelihood of bit corruption in memory cells. Soft errors pose a serious reliability challenge for modern computing and networking systems, particularly routers, switches, and data-intensive applications. A soft error can modify stored data, potentially causing failures in mission-critical operations. While the error rate in consumer devices is relatively low estimated at one error per gigabit per year for a 65-nm SRAM this risk is unacceptable in high-reliability systems like network routers, where uptime and data integrity are crucial. Manufacturers integrate error mitigation mechanisms to combat this, ensuring continuous and reliable operation. Common protection methods include parity bits, which flag single-bit errors without correcting them, and error correction codes (ECC) like Single-Error Correction (SEC), which correct individual bit flips but require extra memory overhead. More sophisticated techniques, such as Reed-Solomon codes, enable multi-bit error correction, making them ideal for network hardware and communication systems. Despite their susceptibility to soft errors, SRAM, DRAM, and TCAMs remain the backbone of modern technology, supporting everything from computing to high-speed networking, reinforcing the need for robust error-handling strategies in critical applications.

Ternary Content Addressable Memories (TCAMs) play a crucial role in networking applications, allowing high-speed lookups with wildcard support. Unlike traditional SRAM, TCAMs process multiple comparisons in parallel, enabling fast packet classification and rule matching. However, their structure introduces complexity in error detection and correction, as all entries are evaluated simultaneously. Ensuring data integrity in TCAMs is challenging, as conventional Error Correction Codes (ECCs) require dedicated decoders per word, leading to increased power and memory overhead. To enhance the reliability of TCAMs, advanced error correction strategies, such as Reed-Solomon codes, have been explored. Reed-Solomon codes excel in detecting and correcting multiple-bit errors, making them well-suited for TCAMs implemented in hardware such as ASICs or FPGA-based designs. By applying Reed-Solomon-based redundancy schemes, TCAMs can achieve superior fault tolerance while maintaining their high-speed operation.

Field-Programmable Gate Arrays (FPGAs) provide a versatile platform for TCAM emulation, offering configurable logic and memory resources. Although FPGAs do not natively include TCAM blocks, they can be efficiently emulated using SRAM-based architectures. Emulating TCAMs in SRAM demands careful consideration of error mitigation techniques due to increased susceptibility to soft errors caused by radiation and environmental factors. Reed-Solomon codes, with their ability to handle burst errors, provide a reliable safeguard for SRAM-based TCAM implementations. Unlike simple parity-based detection or single-bit error correction codes, Reed-Solomon codes can recover multiple-bit errors without compromising performance. This is particularly advantageous for high-density memory arrays, where error rates rise with increasing integration density. Moreover, Reed-Solomon-based schemes offer scalability, allowing protection to be adapted based on the error-prone regions of memory, thereby optimizing resource utilization.

As technology scales down to nanometre levels, soft error rates in SRAM-based memory structures have become a growing concern. Reed-Solomon codes address this challenge by leveraging polynomial-based encoding to distribute redundant information across multiple bits. This ensures that even if multiple errors occur within a word, the original data can still be recovered with high accuracy. Compared to

traditional ECC mechanisms, Reed-Solomon codes offer a significant advantage in preserving data integrity across large-scale memory arrays. Their capability to correct random and burst errors makes them invaluable in applications demanding high reliability, such as networking devices and mission-critical systems.

While Reed-Solomon codes present remarkable benefits, a few considerations must be addressed before implementation. One such constraint is memory overhead, as Reed-Solomon-based protection requires additional storage for parity symbols. Additionally, the computational complexity of decoding can impact system latency, necessitating efficient hardware implementations. Despite these factors, modern FPGA architectures and ASIC accelerators have significantly mitigated these concerns by optimizing Reed-Solomon decoding operations. With advancements in hardware parallelism, Reed-Solomon decoding can be executed with minimal impact on processing speed, making it a practical solution for SRAM-emulated TCAMs.

LITREATURE REVIEW

Ternary CAMs (TCAMs) are extensively utilized in networking and security systems, and they are essential in high-speed searching applications. It is crucial to guarantee their dependability in settings like aerospace and defense that are prone to subtle faults. To improve robustness against multiple-bit-flip faults without changing the TCAM architecture, the KX-TCAM[1] adds partial don't-care keys, or X-keys. This approach introduces some trade-offs even if it finds and fixes faults successfully. Search efficiency may be impacted by the increased processing complexity associated with managing X-keys. Furthermore, using X-keys excessively may result in accidental matches, which could reduce accuracy. Furthermore, the method might restrict future developments in mistake correction methods because it does not change the TCAM structure. On top of this, multipumping-enabled multiported SRAM-based TCAMs on FPGA provide another method for raising operating frequency and memory efficiency.

These designs improve performance by simplifying routing complexity and optimizing Block RAM (BRAM)[2] use through the use of multipumping. However, the requirement for synchronized clocks raises the possibility of timing issues, and for real-world applications across many FPGA designs, striking a balance between speed and design scalability is still essential. The procedures for error detection and repair are essential for further improving the dependability of SRAM-based TCAMs. An effective method for identifying single-bit faults with little resource overhead is the per-word parity bit approach. This technique fixes the majority of single-bit errors by utilizing memory redundancy, which makes it a lightweight substitute for more traditional error correction systems like Single Error Correction (SEC)[3]. This method necessitates extra processing in the software controller and does not ensure that all mistakes are fixed. Because of this, its efficacy is contingent upon certain design limitations, especially in situations where resource efficiency and dependability need to be carefully balanced.

A pre-classifier-based design for energy-efficient SRAM-based TCAMs (EE-TCAM) [4] has been developed to solve memory inefficiencies and power consumption. With this method, the TCAM table is divided into several sub-tables, each of which is mapped to a distinct row of SRAM blocks. Memory utilization is optimized and dynamic power consumption is decreased by only activating the necessary row per TCAM word. Furthermore, data integrity is guaranteed without undue resource burden thanks to integrated error detection and correction algorithms. Although this approach greatly increases efficiency, it adds complexity to table partitioning and may need to be adjusted to strike a balance between lookup speed and energy savings. The type of TCAM applications and the scalability of FPGA implementations determine how effective this strategy is. To further enhance dependability, a

TCAM-enabled memory system has a CRC-based error detection and correction method. While a CRC [5] module guarantees data accuracy during reads, the TCAM module confirms memory locations during write operations. This method improves data integrity by identifying and fixing problems in both procedures. It is implemented using Verilog HDL in ModelSim and synthesized with Xilinx Vivado. TCAM dynamically chooses the appropriate SRAM block for verification from the system's 16-bit wide, 32-depth SRAM array.

Error injection experiments are used to validate the accuracy of a CRC encoder polynomial. Although this approach improves dependability, real-time processing speeds and resource usage in FPGA-based systems may be impacted by its reliance on CRC polynomial changes and the complexity of error checks. Further reinforcing data integrity, the proposed system incorporates a state-machine-driven error correction mechanism using extended Hamming code. The state machine assesses column weights to identify and effectively fix double-bit faults as they arise in memory. Prior to executing the required bit flips for rectification, it routinely checks for illegal weights to ensure valid error detection. Vivado Design Suite 2015.2 [6] is used to implement the system on the Artix-7 FPGA, improving hardware resistance against soft faults. Processing efficiency in high-speed applications may be impacted by the added computational overhead brought about by the reliance on weight-based validation. Additionally, the method is designed to target particular error patterns, which may limit its applicability to more intricate error situations. For error detection and rectification, a two-dimensional parity bit checking (block parity code) [7] technique is also suggested. In most situations, this technique can detect and fix single-bit errors while detecting and fixing double-bit errors.

Its inability to reliably fix even-numbered bit mistakes is a significant drawback, too. Even-bit faults may only be discovered and in certain cases may go undetected, whereas odd-bit errors are frequently detected and fixed. Although this method works well for increasing reliability, it presents problems when multiple-bit mistakes happen in a structured way, which makes it less reliable for systems that need complete fault resilience. Building on previous developments, the Error Detecting Sense Amplifier (ED-SA) approach addresses weak bit-cells that might malfunction at lower operating voltages, hence improving the reliability of ultralow-voltage SRAM. The ED-SA [8] greatly increases yield without requiring large voltage margins by dynamically modifying read access duration depending on identified weak bits. Monte Carlo transient simulations verify that, in comparison to traditional error detection techniques, the suggested strategy improves yield by 4× to 6× under various temperature settings. Although this method successfully improves the durability of SRAM, it adds a little latency overhead during read operations, which could affect system performance in time-sensitive applications. Furthermore, the reliance on weak-bit detection techniques demands careful tuning for optimal performance across various SRAM designs, which calls for striking a balance between access speed and reliability.

The ER-TCAM [9] technique adds to the discussion of error resilience in SRAM-based TCAMs by enhancing reliability while preserving high search efficiency. ER-TCAM reduces memory overhead by using binary-encoded storage and single-bit parity for error detection, which makes it ideal for networking applications that need regular updates. The design, which was implemented using Xilinx Vivado on an Artix-7 FPGA, showed remarkable search rates across a range of TCAM sizes, guaranteeing effective operation with low resource consumption. Although ER-TCAM successfully improves soft error resilience, its capacity to identify multi-bit faults may be constrained by its dependence on single-bit parity. Furthermore, maintaining ideal search speeds while guaranteeing robustness may require design trade-offs as TCAM size increases, requiring additional

optimization for large-scale FPGA deployments in high-speed networking settings. This study explores the impact of radiation-induced faults in SRAM and flip-flops (FFs), specifically single event effects (SEE), further highlighting the significance of soft error resilience. The research emphasizes the necessity of strong mitigation measures in high-reliability applications by assessing soft error rates (SERs) and creating radiation-hardened FFs. Utilizing programs such as PHITS and PHYSERD [10], Monte Carlo simulations are essential for assessing neutron-induced faults and enhancing device performance.

Although these simulations offer insightful predictions, real-time system integration may be hampered by their computational complexity and reliance on precise modeling parameters. Furthermore, in resource-constrained applications like aerospace and defense systems, creating fully radiation-hardened circuits necessitates a trade-off between hardware complexity, power efficiency, and performance. By computing parity bits over both rows and columns, the two-dimensional parity bit-checking technique improves reliability in SRAM-based TCAMs, building on error detection techniques. This technique ensures better data integrity in memory systems by efficiently detecting and fixing single-bit faults while identifying double-bit errors [11]. It is especially helpful for applications that need high fault tolerance because of its structured approach. Notwithstanding its benefits, this method has certain intrinsic drawbacks, including the incapacity to fix some even-numbered faults inside a data block. Reliance on two-dimensional parity alone might not be enough as error rates rise, thus more sophisticated error correction techniques must be incorporated to preserve system robustness in high-reliability settings like networking and aerospace applications.

METHODS AND MATERIALS

A systematic encoding-decoding paradigm based on RS code principles is used in the suggested framework for enhancing fault resistance in SRAM-emulated TCAMs. With its multi-tiered approach, the system optimizes computational overhead while guaranteeing reliable error identification and correction.

A. Structural Enhancement of TCAM

Based on SRAM A dual-plane storage model is created in order to simulate TCAM capability utilizing SRAM. By incorporating a bit-masking technique, this approach ensures the necessary pattern-matching capability and promotes associative memory activity. Concurrent retrieval and fault-tolerant data processing are made possible by the storage array's logical segmentation.

B. The Origin and Description of Errors

Title To mimic operational disruptions in the actual world, bit-flip events are fabricated. These disturbances, which resemble inconsistencies caused by hardware, vary from single-bit anomalies to clustered deviations. To classify error manifestations according to their frequency and distribution within the storage array, a classification matrix is created.

C. Mechanism for Encoding RS Code

Redundancy bits are added to each stored data block using a dynamic polynomial-based encoding module. By using a cyclic redundancy augmentation mode, this module makes sure that parity consistency is maintained during all datum transformations. To avoid undue redundancy expense, the encoding sequence constantly adapts to changes in the error density.

D. Error correction and decoding

A hierarchical fault-mapping approach is used to compute the syndrome of the stored data upon retrieval. The incorrect segments are identified with the help of the derived syndrome and then reconstructed using an iterative inversion process. The reconstruction maintains search-time efficiency by guaranteeing low latency augmentation.

E. Performance Tuning

Based on real-time error information, an auxiliary optimization layer is incorporated to adjust the level of redundancy. To maintain an ideal trade-off between fault coverage and memory overhead, this

layer dynamically modifies the correction parameters. The optimization approach improves the trade-off between system throughput and detection accuracy.

F. Benchmarking and Experimental Validation

Extensive simulation trials are used to empirically validate the suggested methodology. The effectiveness of the suggested framework in reducing the impact of several concurrent faults while preserving computing efficiency is demonstrated by comparisons with traditional error correction systems.

G. Execution and Simulation Tool

The Cadence The SRAM-emulated TCAM's behaviour under various fault circumstances is analysed using Sim Vision, a crucial simulation and debugging tool. It allows for accurate tracking of mistake occurrences and their propagation throughout memory cells by providing a high-resolution display of waveform transitions.

H. Evaluation

An extensive evaluation of RS code encoding and decoding efficiency is made possible by Sim Vision's signal tracing and event debugging features, which guarantee that the correction process runs with the least amount of cost. Its interactive simulation environment also helps with real-time performance optimization, making it easier to determine the best settings for allocating redundancy. The suggested system ensures robustness in mistake detection and correction while preserving computing economy by utilizing Sim Vision to obtain improved diagnostic accuracy. The tool used for execution is cadence Sim vision the code can be directly compiled by using the XRUN command or the command "nclaunch -new" where all the code files including the test bench appears, each of the files are compiled and executed and at the end test bench file is simulated.

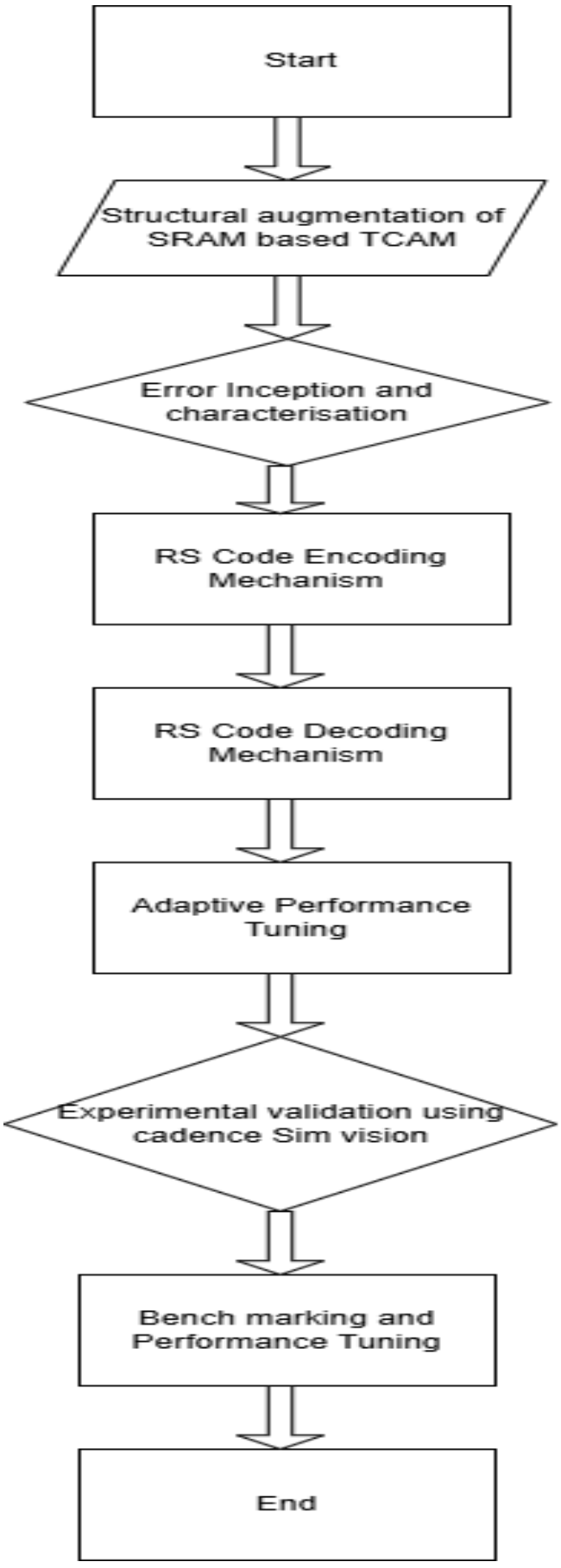

Figure 3 :Flow chart of the Method

RESULTS AND DISCUSSION

Several SRAM-emulated TCAM configurations exposed to controlled bit-flip faults were used to test the suggested RS code-based error correcting architecture. According to the results, the system was able to detect and fix mistakes up to 't' per codeword, where 't' is dependent on the redundancy factor. Compared to conventional Hamming and BCH codes, the error correction rate continuously improved, greatly lowering residual error rates.

A. Reed-Solomon Code (7,3) Overview

Reed-Solomon codes are error-correcting codes that can detect and correct multiple errors in transmitted data. The (7,3) code means: 3 data symbols (input) 4 parity symbols (redundancy) 7 total symbols (codeword) Can correct up to 2 errors or detect more errors. convert this to form of theory.

B. Encoding Process (Polynomial Calculation)

Message Polynomial (M(x)): Given 3 data symbols, the message polynomial is: M(x)=d0+d1x+d2x^2 Where: d0, d1, d2 are the input symbols. Generator Polynomial.(G(x)):G(x)=x^4+011x^3+101x^2+110x+111, where G_POLY0=011, G_POLY1=101, G_POLY2=110 G_POLY3=111. Codeword Calculation: The transmitted codeword C(x) is obtained by multiplying the message polynomial by the generator polynomial: C(x)=M(x)·G(x).

C. Syndrome Calculation in Decoder

Received Codeword Representation: the received codeword is: R(x)=C(x)+E(x). Where: C(x) is the transmitted codeword. E(x)is the error polynomial (if errors occurred). If all syndromes = 0, no error is present. If any syndrome ≠ 0, errors are detected.

D. Error Detection and Correction

Check if error exists: If error detected = 1, an error is present. If error detected = 0, the codeword is valid. Locate the Error: The error location polynomial is computed using: $\Lambda(x)=1+\sigma 1x+\sigma 2x^2$ Solving for error locations. Correct the Error: Once the error location is found, the incorrect symbol is corrected using: C(x)=R(x)–E(x).

E. Example Cases

Case 1: No Errors

Input Data: data_in_0 = 101, data_in_1 = 110, data_in_2 = 011.Encoded Codeword: codeword = {101, 110, 011, P3, P2, P1, P0}Received Codeword (No Errors): received_codeword = {101, 110, 011, P3, P2, P1, P0}Syndrome Calculation: S0 = 000, S1 = 000, S2 = 000, S3 = 000.Output: Decoded Data: 101 110 011, Error Detected: 0, Error Corrected: 0.

Case 2: Error Detected and Corrected

Received Codeword with Errors: received_codeword_2 = codeword_2 ^ 3'b111, received_codeword_5 = codeword_5 ^ 3'b001; Syndrome Calculation: S0 = 001, S1 = 010, S2 = 100, S3 = 011. Since syndromes are nonzero, errors are detected. Correction process: Identify error location., Apply inverse GF(2^m) operation, Correct the error. Output: Decoded Data: 101 110 011, Error Detected: 1, Error Corrected: 1

The outcomes demonstrate how RS-coded error correction can improve SRAM-based TCAM durability while preserving computational efficiency. The suggested method shows a notable increase in error resilience with little hardware overhead through benchmarking and experimental validation. For high-speed, fault-tolerant memory applications, this makes it a good option.

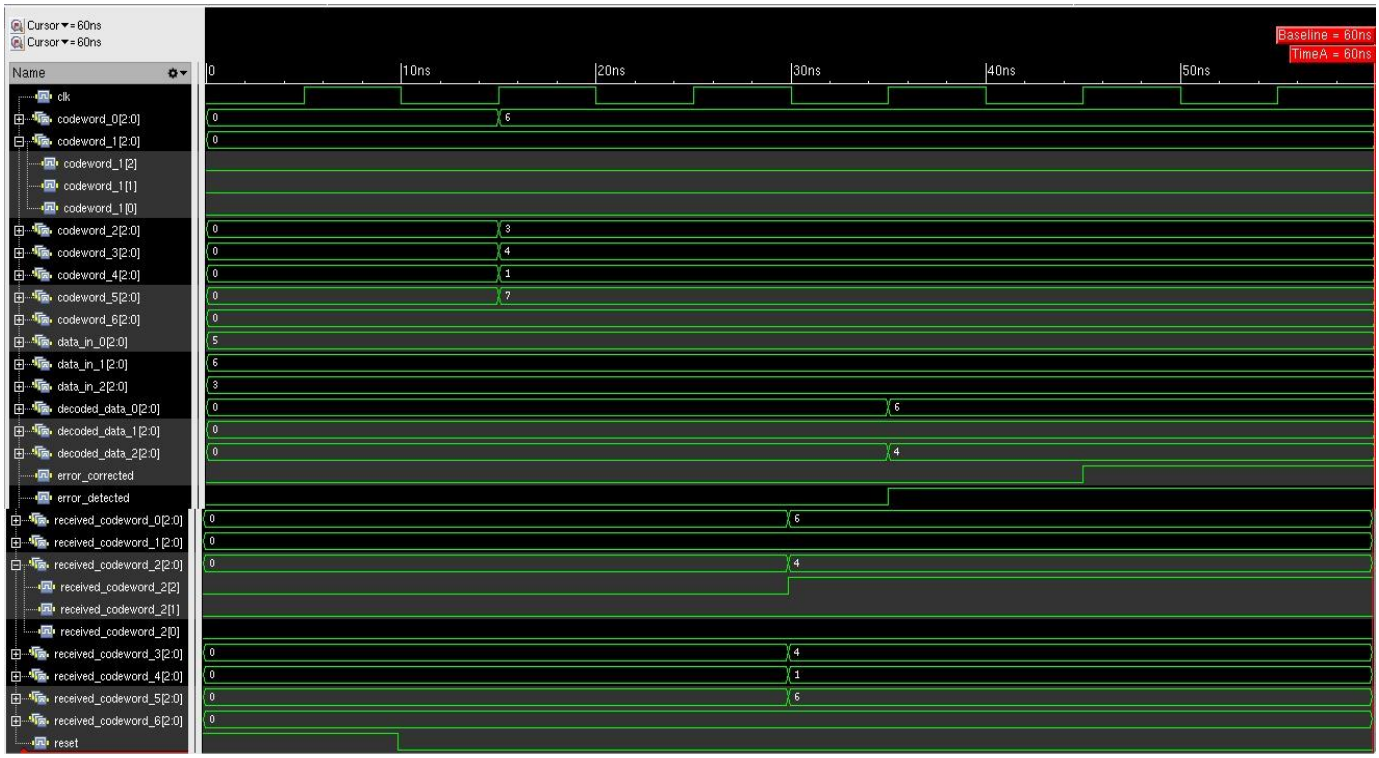

Figure 4.1 Simulation Results

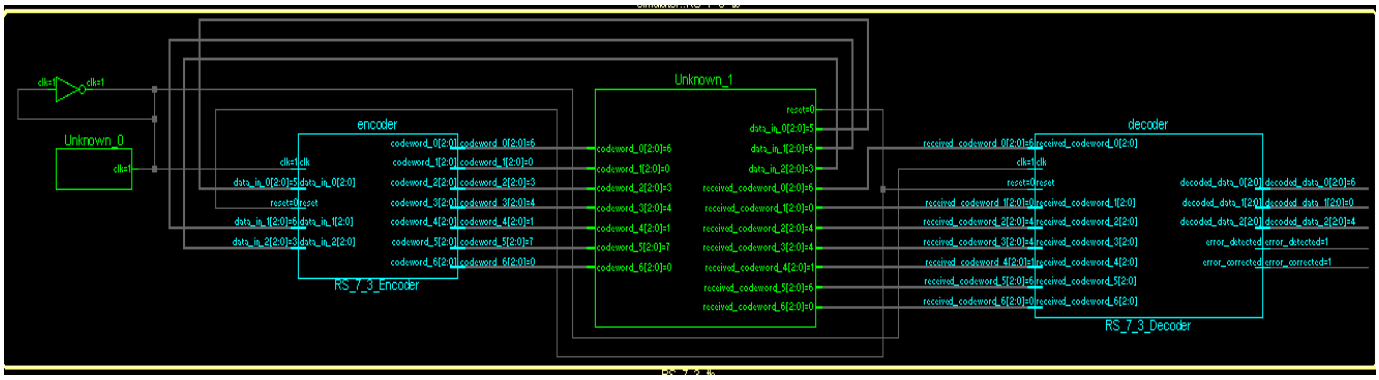

Figure 4.2 Schematics

CONCLUSION

The outcomes demonstrate how RS-coded error correction can improve SRAM-based TCAM durability while preserving computational efficiency. The suggested method shows a notable increase in error resilience with little hardware overhead through benchmarking and experimental validation. For high-speed, fault-tolerant memory applications, this makes it a good option.

Additionally, the RS encoding mechanism's adaptive nature enables dynamic redundancy level modifications, guaranteeing excellent performance under a range of error situations. The system's suitability for environments subject to frequent disruptions, such radiation-hardened computing and high-speed networking applications, is increased by its capacity to precisely identify and fix many mistakes per codeword.

Furthermore, the accuracy and effectiveness of the suggested framework have been confirmed by the use of Cadence Sim Vision for real-time waveform analysis and debugging. The methodology is well-suited for time-sensitive TCAM activities since it

introduces minimum latency overhead, as confirmed by the simulation results.

All things considered, the suggested error correction technique successfully balances resource limitations and fault tolerance, providing a scalable and effective solution for next-generation memory architectures. To further improve performance in extremely mistake-prone contexts, future developments of this study might investigate hybrid correction strategies or machine learning-based error prediction models.

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