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Design and Implementation of a 16 bit ALU in Quantum Dot Cellular Automata

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ABSTRACT

The integrated circuits testing is a time consuming task. In order to get shorter test time, some methods need to develop. This paper presents an original method and a practical system design and implementation of Reverse Logic circuits based Arithmetic and Logic unit (ALU). An ALU is a key factor of this computation process. Digital circuits with reversible multiplexer logic give lesser delay when compared to basic logic gates. The analysis of implemented decoder controlled 16 bit ALU, along with vectored multiplexer selection output is presented here. All arithmetic and logic modules are implemented in reversible logics by which delay is reduced along with power consumption. The designs are implemented and verified in QCAD. The paper aims to provide evidence that QCA (Quantum dot Cellular Automata) has potential applications in future Quantum computers, provided that the underlying technology is made feasible. Design has been made using certain combinational circuits by using Majority gate, AND, OR, NOT, X-OR in QCA.

Keywords : QCA (Quantum dot Cellular Automata), Reversible Gates, ALU (Arithmetic and Logic Unit)

I. INTRODUCTION

A. CMOS Technology

Microprocessor manufacturing processes was governed by Moore's law, and consequently microprocessor performance till now. Today many integrated circuits are manufactured at 0.25-0.33 micron processes. But recent studies indicate that as early as 2010, the physical limits of transistor sizing may be reached however the performance of various circuits in current CMOS-based architectures is close to reaching the limit. If the feature size of transistors is further reduced to a nanometer, it will produce quantum effects such as tunneling. Further, during device scaling process due to the effects of wire resistance and capacitance, the interconnections never scale automatically.

B. An Introduction to QCA Technology

As an alternative to CMOS-VLSI, an approach called the quantum cellular automata (QCA) is developed in 1993 to computing with quantum dots. Unlike conventional computers in which information is transferred from one place to another by electrical current, QCA transfers information by means of propagating a polarization state from one cell to another cell. Hence improving the speed by reduction in area is the main area of research in VLSI system design.

The heart of every computer is an Arithmetic Logic Unit (ALU). This is the part of the computer which performs arithmetic operations on numbers, e.g. addition, subtraction, etc. In digital systems the combinational circuits performs this arithmetic operations. In present VLSI Technology, Power Consumption has become a very important factor for consideration. By using Reversible gates for designing the circuits with reduced power consumption when compared to conventional design based circuits. Reversible Logic finds its own application in Quantum

computing, Nano- technology, optical computing, and computer graphics and low Power VLSI.As having more advantages with reversible logic in digital circuits. The rest of this paper is organized as follows. Section II presents the Reversible concept, Section III presents a review of earlier work, Section IV presents about an ALU with one bit input. Section V describes the proposed 16 bit ALU and finally Section VI gives conclusion.

II. REVERSIBLE LOGIC

The concept of reversible logic gates are used for reducing power consumption and loss of data .This logic uses the reversible gates which have same number of inputs and outputs. Some of the cost metrics like garbage outputs, number of gates, Quantum cost, constant outputs are used to estimate the performance of reversible circuits. A Reversible circuit design can be modeled as a Sequence of discrete time slices and depth is summation of total time slices. In Digital Electronics the binary decoder is a combinational logic circuit that converts the binary integer value to the associated output pattern. Various proposals are given to design of combinational and sequential circuits in the undergoing research. the design of different combinational circuits like binary comparator, Full adder, Full subtractor, Multiplexer circuits using Reversible Decoder is proposed with optimum Quantum cost .The design of different combinational circuits like binary comparator, Full adder, Full subtractor, Multiplexer circuits using Reversible Decoder is proposed with optimum Quantum cost.
The reversible logic gates are:

A. Not Gate:

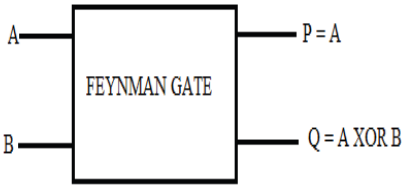
The NOT GATE is the simple Reversible Logic gate. It is 1×1 Reversible Logic Gate with the quantum cost zero. The Not gate simply shifts the complementary of the input to output as shown in the figure1. It is the basic primitive gate which may involve in construction of reversible logic gate, thus owing its own importance in determining the quantum cost of designed Reversible logic gate.

A	P
0	1
1	0

Figure 1. NOT Gate and its Truth Table

B. Feynman Gate (FG)

Feynman gate is a 2×2 reversible gate as shown in below figure2. The Feynman Gate is also called as CNOT gate i.e., controlled NOT gate. The Feynman gate is used to duplicate of the required outputs since Fan-out is not allowed in reversible logic gates. The Quantum Cost of FG is 1. This is also the primitive gate owing its importance in determining quantum cost metric.

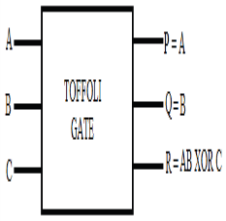


A	B	P	R
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Figure 2. Feynman Gate and its Truth Table

C. Toffoli Gate

(TG): Toffoli Gate is 3×3 reversible gate. The outputs are defined as shown in the below figure3. The Quantum Cost of TG is 4.

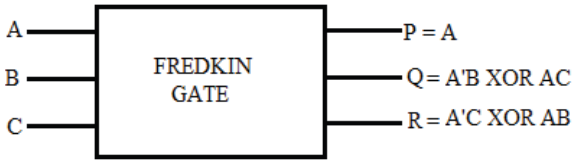


A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Figure 3. Toffoli Gate and its Truth Table

D. FREDKIN GATE (FDG):

Fredkin Gate is a 3×3 reversible gate.

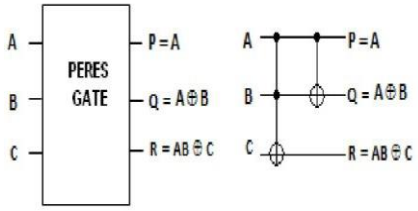


A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Figure 4. Fredkin Gate and its Truth Table

E. *PERES GATE (PG)*

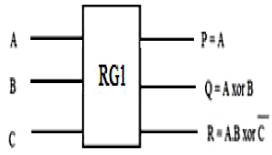
Peres Gate is a 3×3 reversible gate. The outputs are defined as shown in the below figure5. The Quantum Cost of PG is 4.

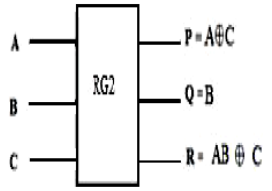


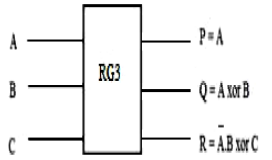
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Figure 5. Peres Gate and its Truth Table

And we use some new reversible gates named RG1, RG2, RG3, and RG4 as given below







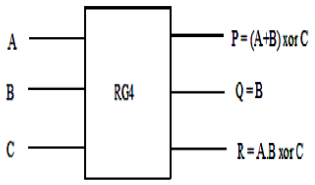


Figure 6. New Reversible gates

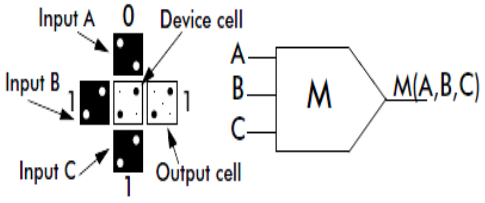
III. EARLIER WORK REVIEW

A. Quantum Dot Cellular Automata

Quantum-dot cellular automata is a computing paradigm using arrays of nanostructures called quantum dots Quantum dots are nanostructures created from standard semi conductive materials such as *Si/SiO2*. These structures can be modeled as 3-dimensional quantum wells. As a result, they exhibit energy quantization effects even at distances several hundred times larger than a material's lattice constant.

Quantum cellular automata (QCA) is a new technology in nano meter scale (<18nm) to support nanotechnology. QCA is very effective in terms of high space density and power dissipation and will be playing a major role in the develop-pment of the Quantum computer with low power consumption and high speed. And a Quantum Dot cellular Automata (QCA) is an emerging technology that takes advantage of quantum effects, which become increasingly apparent at the scale of a few nanometers.

The QCA cell [9] consists of a system of four quantum dots charged with only two free electrons. Electrostatic repulsion between these electrons force them to occupy only the diagonal sites creating a so called "polarization" used to encode binary information.
In QCA all the Logic Operations are must be generated with Majority Logic Gate only. The structure of majority gate is given below



A	B	C	M
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Figure 7. Majority gate in QCA and its truth table

B. QCA Clocking

The clocking of QCA is accomplished by controlling the potential barriers between adjacent quantum-dots. When tunneling potential is high the electron wave functions become de-localized causing indefinite polarization. Raising the potential barrier decreases the tunneling potential, as a result the electrons begin to localize. Once the electrons localize the cell gains a definite polarization.

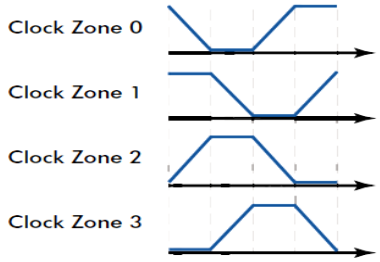


Figure 8. QCA clock zones

C. ALU Architecture

The Arithmetic Logic Unit (ALU) performs the basic arithmetic and logical operation. The ALU consists of arithmetic extender, logical extender and a Multiplexer which is shown in Fig. 9 below. The control signals will decides the operation of the ALU. And also one mode control input which select between arithmetic and logical operations.

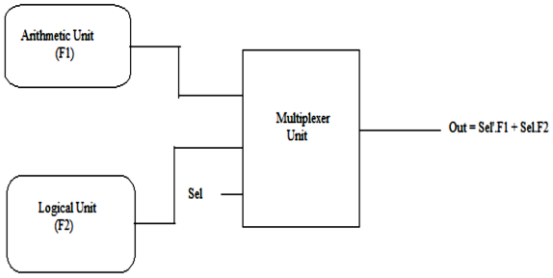


Figure 9. Structure of ALU

IV. PROPOSED ALU DESIGN

In the Processor architecture the ALU is considered as the heart of the system. An arithmetic and logical unit should be capable of producing larger number of possible arithmetic and logic functions. Based on the reversible gate structure the ALU design can be made remarkably, the reversible gates should maximize the operations of arithmetic and logical unit. But the cost of the circuit select lines used for designing the circuit garbage outputs of the circuit design, circuit delays must be reduced, to ensure this at each stage verification should be made whether the reversibility is present in each and every part of the design and the outputs should propagate in a manner to achieve the correct operation of the circuit and also to achieve reversibility of the design

A. Proposed Arithmetic Unit

The Arithmetic unit is responsible for handling the arithmetic operations executed by the program. The proposed arithmetic unit is designed based on the novel reversible gates

Control Inputs			Output	Results
C_0	C_1	C_2		
0	0	0	B	Transfer B
0	0	1	B+1	Increment B
0	1	0	A + B	Addition
0	1	1	A + B + 1	Addition with carry
1	0	0	A + B	1's complement subtraction
1	0	1	A + B + 1	2's complement subtraction
1	1	0	B-1	Decrement B
1	1	1	B	Transfer B

The output function is realized based on the equation below

$$F1 = (AC_0 + AC_1)\ xor\ B\ xor\ C_2$$

Where A, B are the inputs given to the reversible gates and C0, C1, C2 are the control inputs.

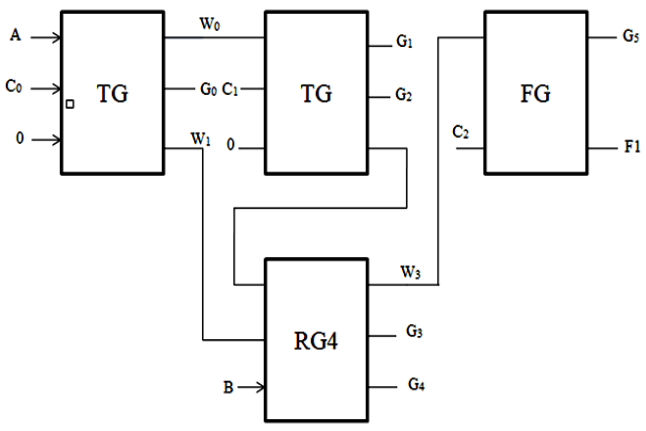


Figure 10. AU Design

B. Proposed Logic Unit

The Logical unit is the another important constituent in the Central Processing Unit as it is responsible for handling the logical operations executed by the programmer. The proposed design of logical unit design is based on the novel reversible gates.

Control Inputs				Output	Results
C0	C1	C2	C3		
0	0	0	0	0	-
0	0	0	1	A.B	AND
0	0	1	0	B	COPY
0	1	0	1	A	COPY
0	1	1	0	A xor B	XOR
0	1	1	1	A+B	OR
1	0	0	0	(A+B)'	NOR
1	0	0	1	(A xor B)'	Equal
1	0	1	0	A'	NOT
1	1	0	0	B'	NOT
1	1	1	0	(A.B)'	NAND
1	1	1	1	1	Constant

The functionalities of Logical unit can be designed by the output equation as follows

$$F2 = A'B'C_0 + AB'C_1 + A'BC_2 + ABC_3$$

The value of C0,C1,C2,C3 is taken as the control inputs based on the control input values that is by changing the inputs combinations of 0's and 1's the respective logical functions can be obtained.

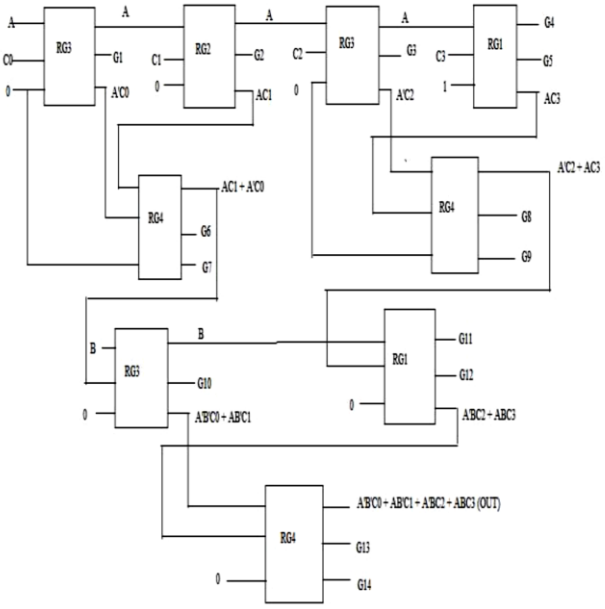


Figure 11. LU Design

V. DESIGNS AND IMPLEMENTATIONS

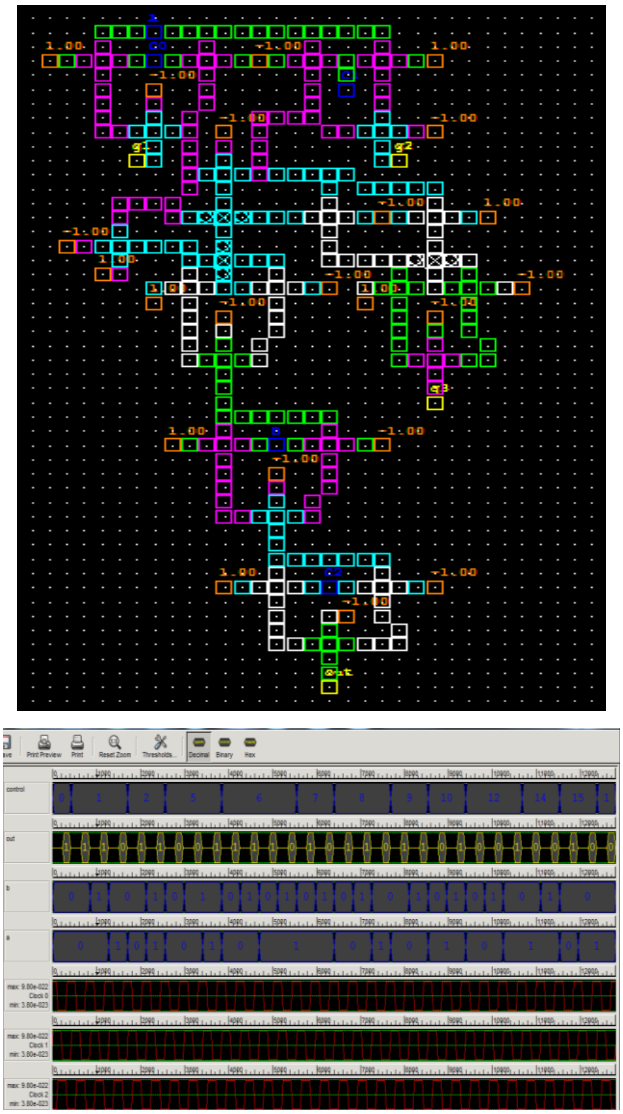
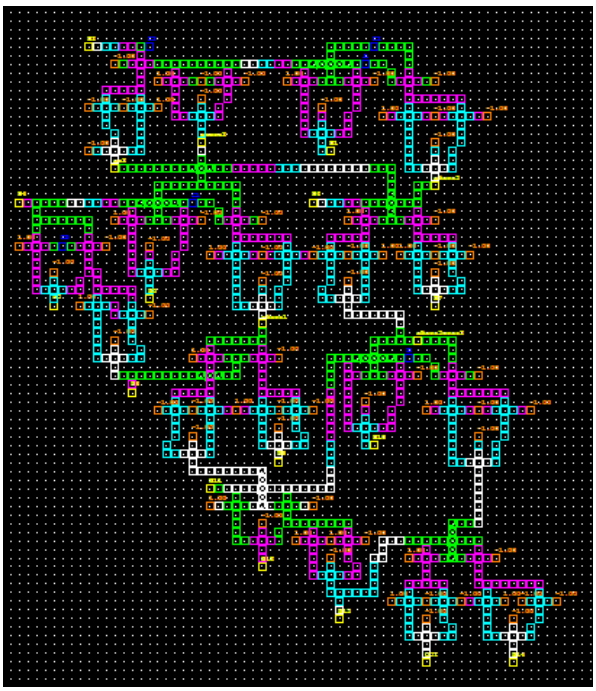


Figure 12. AU Design and simulation result



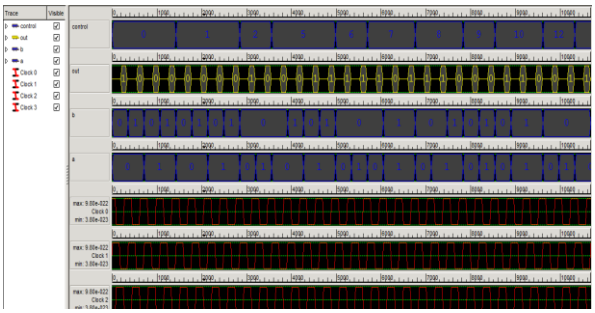


Figure 13. LU Design and Simulation Result

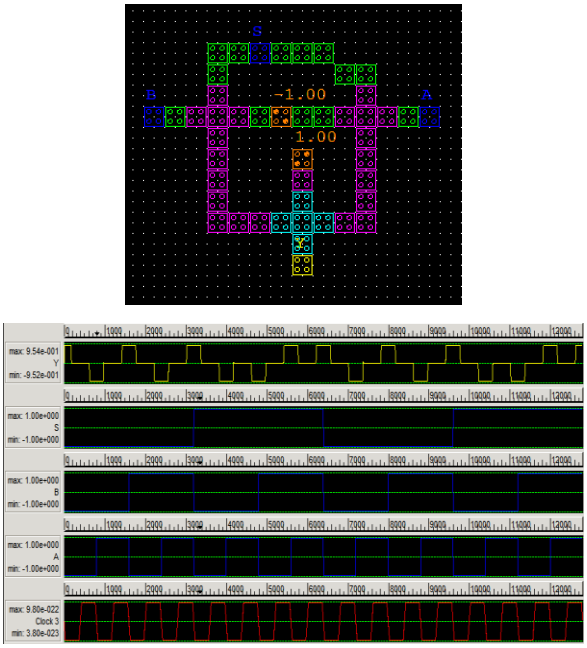


Figure 14. Multiplexer design and simulation result

16 bit ALU

An ALU is designed by making the design with AU and LU by using a multiplexer

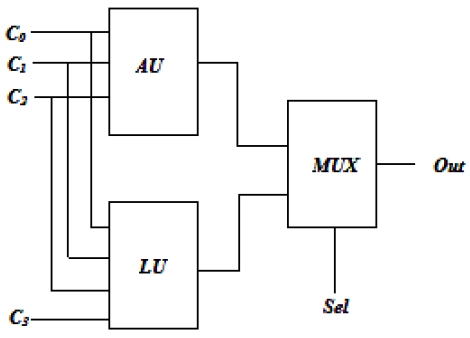


Figure 14. ALU design

VI.CONCLUSION

The proposed gates show improvement in terms of optimization parameters in reversible logic as compared to the existing reversible gates. The Arithmetic and Logic Unit is designed using the proposed gates. The design is validated in the QCA platform. The proposed 16 bit arithmetic and logic unit shows prodigious improvement in the design parameters of reversible logic and the simulation constraints such as area, simulation time and number of cells employed in the design. Hence the proposed system has minimum area with QCA and low power dissipation with Reversible Logic.

VII. References

[1] C.H. Bennett, “Logical Reversibility of Computation”, IBM J.Researchand Development, pp. 525-532, November 1973.

[2] C H Bennett, "Notes on the History of Reversible Computation", IBMJournal of Research and Development,vol. 32, pp. 16-23, 1998.

[3] A. Peres, “Reversible logic and quantum computers”, phys. Rev .A,Gen.Phys., vol. 32, no. 6, pp. 32663276, Dec. 1985.

[4] J. Rajski, J. Tyszer, M. Kassab, and N. Mukherjee, ``Embedded deterministic test," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 23,no. 5, pp. 776_792, May 2004.

[5] Brglez, D. Bryan, K. Kozminski, "Combinational Profiles of sequential benchmark circuits", *Proc. IEEE ISCAS*, pp. 1929-1934, 1989.

A. S. Abu-Issa and S. F. Quigley, “Bit-swapping LFSR and scan-chainordering: A novel technique for peak- and average-power reduction in scan-based BIST,” *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 28, no. 5, pp. 755–759, May 2009.

[6] V. D. Agrawal, C. R. Kime, and K. K. Saluja, “A tutorial on built-in selftest.I. Principles,”

IEEE Des. Test Comput., vol. 10, no. 1, pp. 73–82,Mar. 1993.

[7] J. Rajski, J. Tyszer, G. Mrugalski, and B. Nadeau-Dostie, "Test generatorwith preselected toggling for low power built-in self-test," in *Proc. Eur.Test Symp.*, May 2012, pp. 1–6.

[8] Y. Sato, S. Wang, T. Kato, K. Miyase, and S. Kajihara, "Low powerBIST for scan-shift and capture power," in *Proc. IEEE 21st Asian TestSymp.*, Nov. 2012, pp. 173–178.

[9] K. Moghaddam, J. Rajski, M. Kassab, and S. M. Reddy, "At-speedscan test with low switching activity," in *Proc. IEEE VLSI Test Symp.*,Apr. 2010, pp. 177–182.

A. Peres, "Reversible logic and quantum computers",phys.rev.A,Gen.Phys., vol. 32, no. 6, pp. 32663276, Dec. 1985.

[10] H.G Rangaraju, U. Venugopal, K.N. Muralidhara, K. B. Raja,"Lowpower reversible parallel binary adder / subtractor" arXiv.org/1009.6218,2010.

[11] J.M. Rabaey and M. Pedram, "Low Power Design Methodologies,"Kluwer Academic Publisher, 1997.

[12] T. Toffoli., "Reversible Computing", Tech memo MIT/LCS/TM-151,MIT Lab for Computer Science 1980.