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Design of High Performance CMOS Current Comparator

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ABSTRACT

This paper exhibits a two regular Current Comparator configuration are recreated in various innovation. The one comparator configuration depends on positive criticism types and another is on wilson current mirror with pMOS gadget. The circuit execution are effectively contrasted and parameter like proliferation delay, balance voltage and power scattering. Additionally, the ordinary comparator configuration dependent on wilson current mirror is altered in two different ways. In one adjusted circuit the Wilson current mirror is change from pMOS to nMOS. While in another comparator structure the Wilson, current mirror is supplanted by basic/standard current mirror. These comparator configuration gives better outcome with contrasted with ordinary comparator as far as spread deferral and balance voltage.

Keywords : Analog CMOS Circuit Design, Current Comparator, Positive Feedback, Low Power, High Speed.

I. INTRODUCTION

The general trend in CMOS technology is to make the devices smaller and smaller. By this the density and speed of digital circuits increases. Also, by reducing the thickness of the gate oxide, the driving capability of the transistor is too much increases. In addition, the thickness reduction implies that the supply voltage must be decreased to avoid excessive electric field in the devices.

Three main reasons can be given for the advent of low-voltage circuits. As the channel length is scaled down into sub-microns and the gate-oxide thickness becomes only several nanometers thick, the supply voltage must be reduced in order to ensure device reliability. The second reason emanates from the increasing number of components on a single chip. A silicon chip can only dissipate a limited amount of power per unit area. Since the increasing density of components allows more electronic function per unit area, the power per electronic function must be lowered in order to prevent overheating of the chip. The third reason is directed by portable, battery-powered equipment. In order to have an acceptable operation period from a battery, both the supply power and the supply voltage must be reduced.

The comparator compares analog signal with another analog signal or reference and outputs a signal based on the comparison. The comparator is widely used in the process of converting analog signal to digital signals. It is an important device widely used in Analog to Digital Converter (ADC). Among the many architectures of ADC, Sigma delta, designs are used in a large class of applications ranging from low frequency and audio to down converted intermediate frequency and digital video .Their property to Trade speed for accuracy makes them more attractive in the context of present CMOS technology evolution.[1]

Low power and high-speed comparators are the main building blocks in the front-end of a radio-frequency receiver in most of the modern telecommunication systems. The ever-growing application of portable devices makes the power consumption a very critical constraint for circuit designers. Comparators are used in ADCs, data transmission, switching power regulators, and many other applications.

The comparator design plays an important role in high speed ADCs. Power consumption and speed is key metrics in comparator design. For all high speed ADCs, regardless of the architecture, one of the critical performance limiting building blocks is the comparator, which in large measure determines the overall performance of data converters, including the maximum sampling rate, bit resolution, and total power consumption.[2]

1. Existing Architectures of Differential Dynamic Comparator

The ideal current comparator is a device that can do two main things extremely well. First, once a signal is applied it can react to the signal instantaneously, and second, its output reaches its zenith at the same that the device reacts to the input signal. To build an ideal current comparator, one would ideally have a device which would allow the input signal to settle very quickly, i.e. there would be no capacitance on the input and it would be able to take an infinitely small change in current and convert it into a N1 scale change in voltage at the output of the device. This would result infinite trans impedance gain as shown in this equation:

$$Rtran = \frac{\Delta Vout}{\Delta Iin} \quad (1)$$

Unfortunately, real devices use real components with real input capacitances, and a finite trans-impedance gain is ail that can be achieved. So when designing a current comparator one wants to build a device with high gain so that the transition time is as fast as possible and where the input impedance is as low as possible so that the signal settles quickly.

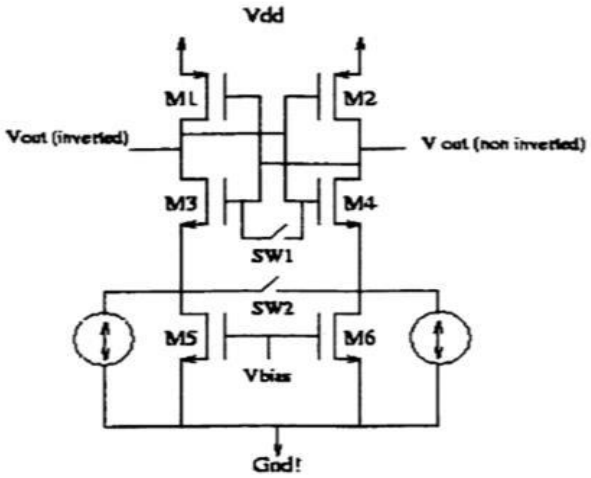

Fig 1. First experiment in high speed current comparison

The first novel design comes from a device which is used solely as a bit line comparator, i.e., limited current range and high speed for use as a bit line sense amplifier for RAM chips [3]. This design had some very promising features, such as almost constant comparison time for ail current differences, simple and compact design, incredibly high speed, and low power with a time differential input. A circuit diagram of the chip is shown in Figure 3.2. This device operates by first closing SW1 and SW2 to balance the device- Then the current sources are applied differentially across SW2, then SW2 and SW1 are opened sequentially and the device quickly settles to the resultant value.

2. Proposed Comparator

Different methods of correcting for the matching errors were attempted with only modest improvements in performance. Several different designs were attempted with the best of these submitted for testing in a CMOS fabrication run- By the time the fabricated chip was received, it was decided that pursuing this design was ill fated and

thus the pursuit of a different design based on a leading current comparator was undertaken. The former design required some complex timing and also did not satisfy a low supply power design methodology, so a new design based on a different approach similar to the leading comparator was attempted.

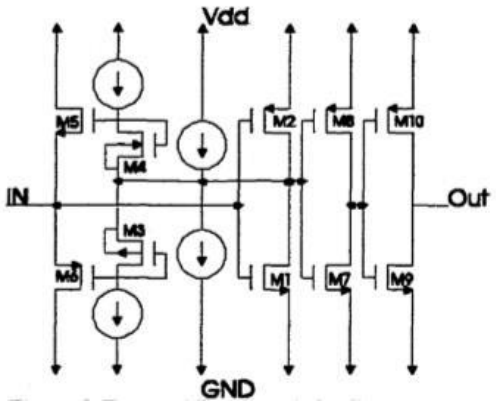

Figure 2. Tang and Toumazou's leading current comparator

2.1 Operation of the Proposed Comparator

First the circuit was simulated using HSPW291 to determine its characteristics. This led to the early identification of a problem associated with charge injection at the higher current levels when the switches which clamp the balanced unstable output devices opened. Different methods of controlling this problem were attempted to try and improve the performance of the design such as half sized dummy switches, but with limited success. At this time it was noted that a much greater problem plaguing the performance of the design was that matching associated with standard CMOS processes retards the performance of this method to no better than middle of the class.

2.2 Performance Analysis and Design Trade-Offs

The new design is shown in Figure 3.2. This new design has several beneficial features: the input voltage level can be set by controlling Vbias, the twin tub process is no longer required for fabrication, it theoretically operates at lower voltages than "Tang and Toumazou" ,and initial simulations, using the Norte1 BiCMOS transistor model, showed a higher operating speed.

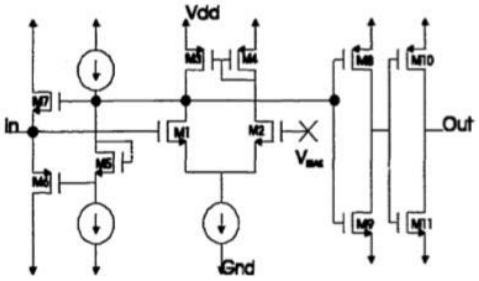

Figure 3. The novel current comparator

2.2.1 Offset Analysis

Input offset voltage can be classified as two types. (i) Systematic offset and (ii) Random offset. Offset in the Comparators generates due to input transistor mismatches (i.e. mismatches in the threshold voltages and mismatches in the trans-conductance parameter $\beta=\mu Cox\ W/L$. The output changes as the input differences crosses zero as shown in Figure 4.3.If the output did not change until the input difference reached a value Vos then this difference would be defined as the offset voltage shown in Figure 3.3.

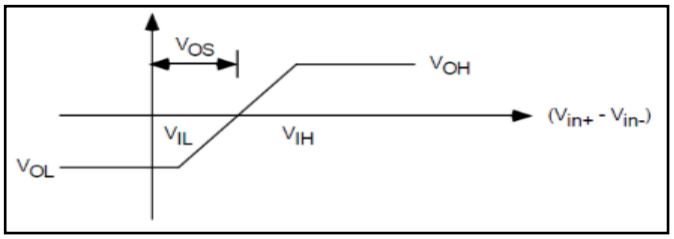

Figure 4. Transfer curve of the comparator including input-offset voltage [11]

This would not be a problem if the offset could be predicted, but it varies randomly from the circuit to circuit for a given design. The sign of Vos is unknown in polarity. The offset voltage can be formally defined as the input level which forces the output voltage to go to zero. It can limit the resolution of the

comparator, thus adversely affecting the accuracy of the comparator and the ADC it is used in.

2.2.2 Delay Analysis

The decision stage is the heart of this comparator and is used to determine which of the input signals is larger (i.e. should be capable of discriminating mV level signals). The schematic of the decision stage of the comparator is shown in the figure 4.8 below. This circuit uses positive feedback from the cross-gate connection of M6 and M7 to increase the gain of the decision element. Hysteresis can be part of the design in the decision circuit.

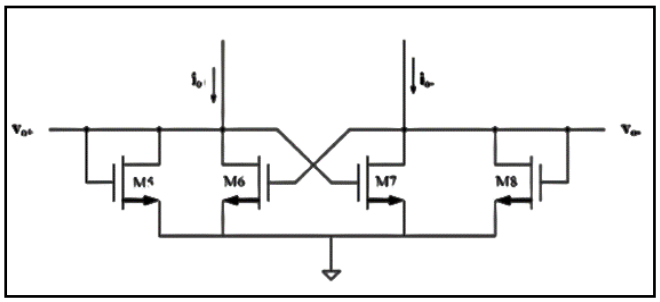

Figure 5. Positive feedback decision circuit

Assuming that io+> io-, M5 and M7 are on and M6 and M8 are off. Also assume that β5= β8= βA and β6 = β7= βB where β5, β6, β7, β8 are the trans-conductance parameters of the transistors M5, M6, M7 and M8 respectively. Under these assumptions Vo(-) is 0approximately 0 V and Vo(+) is,

$$\mathbf{Vo}\ (+) = \sqrt{\mathbf{2} * \frac{\boldsymbol{i0(+)}}{\boldsymbol{\beta A}}} + \boldsymbol{V_{TH}}$$

If io- is increased and io + is decreased, switching takes place when the drain-source voltage of M7 is equal toVth of M6. So M6 turns on and M7 shuts off. At this point, io- is given by,

$$\boldsymbol{i_O}\ (\mathbf{-}) = \frac{\boldsymbol{\beta B}}{\boldsymbol{\beta A}} * \boldsymbol{i_O}\ (+)$$

A similar analysis for increasing io+ and decreasing io- yields a switching point of

$$\boldsymbol{i_O}(-) = \frac{\boldsymbol{\beta B}}{\boldsymbol{\beta A}} * \boldsymbol{I_O}\ (-)$$

II. SIMULATION RESULT

The conventional circuit of CMOS Current comparator is simulated in TSMC 180nm CMOS process technology. The performance of circuit is simulated and compared for different input current pulse. The circuit performance is evaluated in terms of propagation delay and power dissipation. The inverter M5/M2 begins to switch as the voltage on the comparator node is affected by input current. As soon as this slews to either rail, the transistors M0 or M6 are switched open and then with a delay of about10 ns the transistors M1 or M7 respectively are switched closed.

2.3. Simulation Results in TSMC 180nm Technology

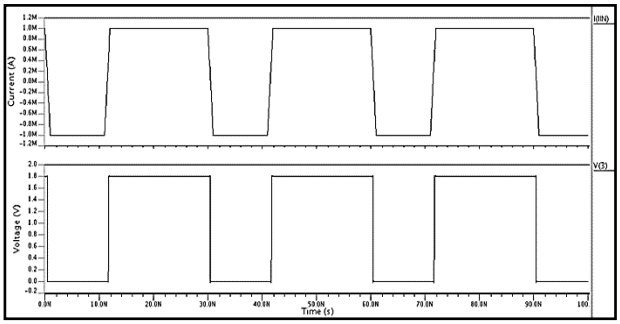

Figure 6. Transient analysis for input current pulse ±1mA

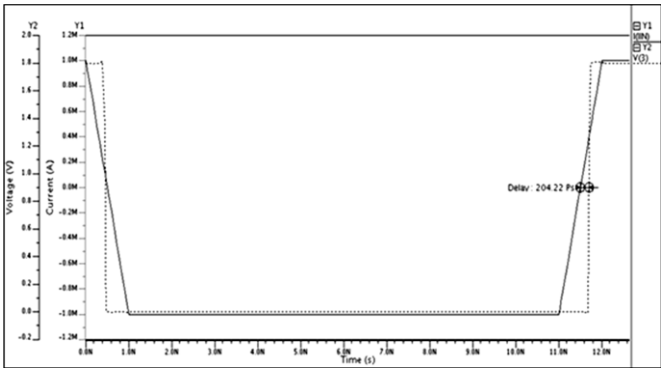

Figure 7. Propagation delay for input current pulse ±1mA

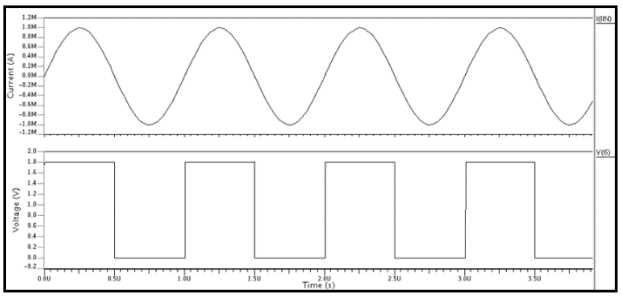

Figure 8. Sine-wave as Input Signal

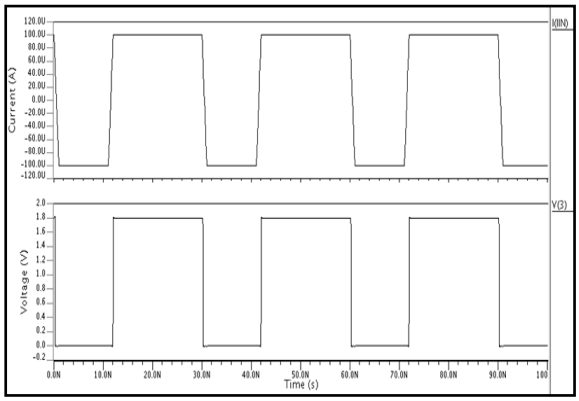

Figure 9. Transient analysis for input current pulse ±100μA

Table 1. Comparison of Different Current Comparator TSMC 180nm Technology

Parameters	Wilson Current Mirror based Current Comparator	Modified Comparator Design:1	Modified Comparator Design:2
Propagation Delay(Ps)	411.26	209.07	362.8
Speed(GHZ)	2.4	4.7	2.7
Offset(mV)	40.04	32.43	36.04
Power Dissipation (μW)	8.6	24.71	18.29

Table 2. Comparison of Different Current Comparator Generic 130nm Technology

Parameters	Wilson Current Mirror based Current Comparator	Modified Comparator Design:1	Modified Comparator Design:2
Propagation Delay(Ps)	370.79	189.65	318.1
Speed(GHz)	2.7	5	3.1
Offset (mV)	20.30	19.92	33.87
Power Dissipation (μW)	8.1	0.68	15.46

III. CONCLUSION

In this task, CMOS current comparator different traditional current comparator are recreated to accomplish fast and low balance as a writing review. The comparator depends on positive input type comparator, Wilson current mirror-based comparator are effectively considered and mimicked. The reenactment is done in TSMC 180nm, Generic 130nm and Generic 90nm CMOS process innovation. Likewise, reproduction result is very much thought about for all technology. For recreation here SPICE test system is utilized.

Likewise, the comparator configuration is changed in part 6 for accomplishing fast and low balance voltage to satisfaction the title of this venture. The changed hardware is recreated in TSMC 180nm, Generic 130nm and conventional 90nm innovation. Toward the end relative examination of all circuit are accomplished for various innovation.

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