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Impact of Automation on the Test Insertion

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ABSTRACT

In the present scenario, the transistor size (channel length) is diminishing which has led to number of irregularities and manufacturing defects. Thus the testing of the manufacturing defects in an IC is very important. In this paper, we are presenting the impact of the flow automation on the test insertion. We have performed the test insertion through an automated flow for 28nm and 16FF test cases.

Keywords : Built in Self-Test, Design For Testability, Scan, Test Automation.

I. INTRODUCTION

Design for Testability is a design technique that adds certain testability features in the digital modules. The idea of the added features is that they make it easier to develop and apply manufacturing tests for the designed hardware.

The purpose of manufacturing tests is to validate that the product hardware contains no defects that could, otherwise, adversely affect the product's correct functioning.

Tests are applied at several steps in the hardware manufacturing flow. The tests generally are driven by test programs that execute in Automatic Test Equipment (ATE). In addition to finding and indicating the presence of defects (i.e., the test fails), tests may be able to log diagnostic information about the nature of the encountered test

fails. The diagnostic information can be used to locate the source of the failure.

In other words, the response of vectors (patterns) from a good circuit is compared with the response of vectors (using same patterns) from a DUT (device under test). If the response is the same or matches, the circuit is good. Otherwise, the circuit is faulty.

DFT plays an important role in the development of test programs and as an interface for test application and diagnostics. Automatic test pattern generation, or ATPG, is much easier if appropriate DFT rules and suggestions have been implemented.

Design for testability (DFT) makes it possible to:

- Assure the detection of all faults in a circuit.
- Reduce the cost and time associated with test development.
- Reduce the execution time of performing test on fabricated chips.

II. METHODOLOGY

The process of test insertion for checking the manufacturing faults is carried out as follows:

• Initially, the functionally verified timing closed netlist is passed through the process of BIST insertion for the memories, where the BIST engine produces the test pattern for the checking the correct working of memory elements. The Basic BIST

Architecture consists of the following components

Test pattern generator (TPG): Responsible for generating the test vectors based on the algorithm implemented, to cover the maximum faults[2].

Test Controller: Responsible for controlling the BIST components for self-test. It signals when BIST start and looks after the comparator, whether it is correctly comparing the right patterns. It finally signals the end of test and signals whether the memory has passed the test based on the ORA.

Output Response Analyzer: Responsible for signaling whether the memory is faulty or not. This is shown in Fig 1

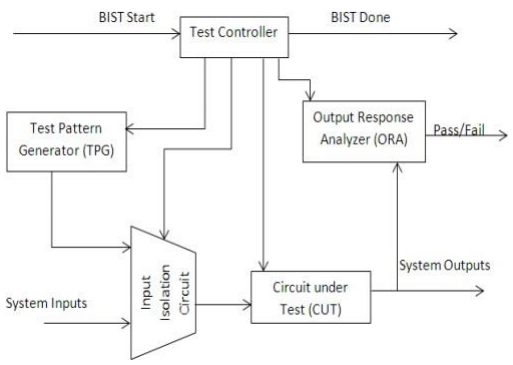

Fig. 1. BIST Architecture

This BIST insertion flow will produce a wrapper around the memory, processor to control the algorithm working, e-fuse which will contain the information regarding the repair that has to be performed. It also generates the server which will synchronize the operations of many processors.

• The BIST related Pins are pulled to the top level so that the test pins are controllable.

• The BIST Inserted Design is carried through the process of scan Insertion of Scan Insertion and Scan Stitching.

• Scan insertion with hierarchical flow: we will insert the scan flops(flops with a multiplexer at D Pin) as shown in the Fig 2.[2] This scan flops provide controllability and observability to the nodes from the top level. We will be using the core wrapped flow where the scan chains are differentiated into core scan chain and wrapper chain. [3]

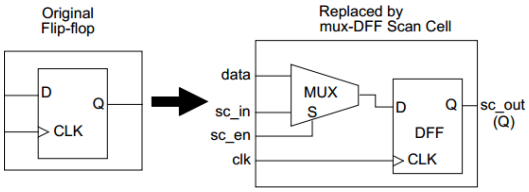

Fig.2. Scan Flop

Scan stitching: In this stage, stitching of scan flops inserted in the previous step is done. Here the scan stitching depends on the constraints given by the user such as maximum chain length, number of input channels and output channels etc.[5]

• Verification of test Insertion: we will generate the test patterns using the ATPG, which will be used for the detection of faults, which will be used for the verification of fault and test insertion.

III. ANALYSIS AND RESULTS

Designs need to be more test-friendly. Far too often, test is sacrificed for some other design criterion like speed, area and power. The design lacks the available resources to adequately address test issues up front, where their impact is felt least .More and more, problems in time-closure and testability cause a far greater resource and schedule impact than is saved by not addressing DFTA (design for test automation) issues during a design's initial development. By deferring complete test consideration until when the design is handed to test insertion flow, it is often too late to change the design the problem shifts

from a development group's design problem to a recurring nightmare for those involved in test-compliance and timing closure in the backend.

The impact non-DFTA compliance is felt with every ASIC that does test differently or incorporates components that are not DFTA- ready[4].

The consequences are quite costly if a non- DFTA-compliant design is accepted for signoff. It may lead to

- Poor test coverage.
- The result was that every design implemented test differently. The effort required to get through signoff was seldom known, with potential problems at any step. This leads to increased signoff effort.
- Error-prone not every nuance of a design could be verified to be correct if no standard existed with which to reference a design's compliance.
- Tasks repeated many times throughout the flow were bound to deviate ever so slightly from the way they were done before.
- Incorrect test structure connectivity, improperly executed test vector generation, and inadequate test coverage contributed to many protoholds and lost time.

The test insertion flow is shown in the Fig. 3.below

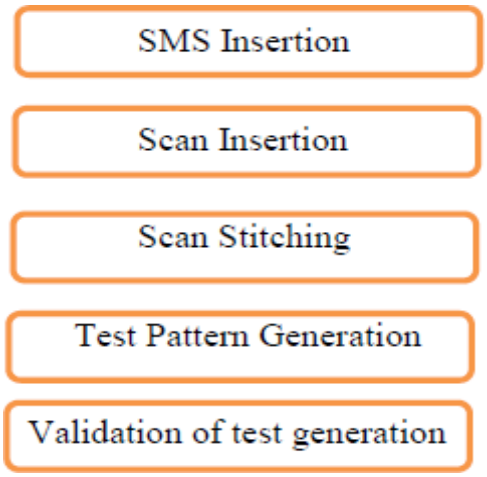

Fig. 3.Test Insertion Flow

The automated flow provides the following advantages like:

- This flow provides the architecture for the RTL based as well as Gate level design for insertion of test elements
- Enhanced architecture to have both ATE test and in-system test interface to be similar
- Overall reduced validation effort
- Utilize third party tool capabilities as much as possible.
- Complete Hierarchical DFT Implementation.
- Utilize standards IEEE P1500 for IP Test and SMS test[6].

Insertion of the test circuitry is carried out at the block level and top level for different test cases using an automated flow. Results Analysis is shown in the table below:

Testcase 1: two hard-macros are instantiated in the top level and no memories at the top level.

Testcase 2: two hard-macros along with large number of memories (with different configurations) are instantiated at the top level.

The run-time and memory utilization for the automated flow is as follows:

Testcase1:

Different stages of the flow	Run-time (in minutes)	Memory Required (in KB)
SMS Insertion	16	203316
TLI 1	11	883712
Scan Insertion	7	113489
TLI 2	11	902144
Scan Stitching	18	201578

Testcase 2:

Different stages of the flow	Run-time (in minutes)	Memory Required (in KB)
SMS Insertion	1470	127688788
TLI 1	145	30382404
Scan Insertion	140	27688788
TLI 2	211	64946176
Scan Stitching	1530	127762192

Block level (hard-macro)

Different stages of the flow	Run-time (in minutes)	Memory Required (in KB)
SMS Insertion	20	12304913
TLI 1	4	1002496
Scan Insertion and stitching	25	12600538
TLI 2	2	1019904

IV. CONCLUSION

This automated flow provides good test coverage and also provides standard methodology. The TAT (Turnaround Time) of the flow has to be enhanced. Also, the memory consumption by the individual stages of the flow is to be optimized.

V. REFERENCES

[1] D.Vamsikrishna, Area analysis of 16 FinFET SRAMs" in National level Technical Symposium, Sri Shirdi Sai Engineering College, Bangalore.

[2] Laung-Terng Wang , Cheng-Wen Wu , Xiaoqing Wen, VLSI Test Principles and Architectures: Design for Testability (Systems on Silicon).

[3] Scan and ATPG Process Guide, Mentor graphics.

[4] FAST User Guide, LSI Internal Tool Guide.

[5] Jing Ye and et all, "Diagnosis and Layout Aware (DLA) Scan Chain Stitching" in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015 | Volume: 23, Issue: 3

[6] K. Katoh ; A. Doumar ; H. Ito, "Design of on-line testing for SoC with IEEE P1500 compliant cores using reconfigurable hardware and scan shift", 11th IEEE International On-Line Testing Symposium, Year: 2005