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Performance Analysis of Fully Differential Double Tail Dynamic Comparator

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ABSTRACT

This paper presents a novel fully differential double tail dynamic comparator that exhibits lower offset voltage than the conventional dynamic comparators. This paper comprises a novel fully differential double tail high performance comparator suitable for low-voltage low-power applications. A fully differential double tail comparator has been designed to meet the necessity of low offset voltage for optimum power with high speed. The expression for the calculation of the offset voltage of the proposed comparator is derived. These expressions corroborate previously stated results with analytical support as well as providing useful insight for the design of fully differential double tail dynamic comparator by analyzing the influence of each transistor pair individually. Transistor mismatch analysis is carried out for offset voltage to fully explore the trade-offs in the design of comparator. In proposed comparator offset voltage is significantly reduced for optimum power. Authors have proposed novel architecture of dynamic voltage comparator which is differential and double tail and verified the architecture by simulation in 180nm CMOS technology with ±0.9V supply. The Post-layout simulation results illustrates that a comparator designed with the proposed techniques is 45% faster, and 30% more power efficient and exhibits 91% low offset as compared with conventional comparator, which is the fastest among the conventional comparators.

Keywords : Comparator, Differential Dynamic Comparator (DDC), Fully Differential Double Tail Dynamic Comparator (FDDTDC), Analog to Digital Converters (ADCs), Propagation delay, Offset Voltage, Power Dissipation.

I. INTRODUCTION

The incredible demand for high performance ADC is pushing towards the use of dynamic comparator to maximize speed and to optimize the power. In most of all ICs, a significant component called ADC, that bridges the gap between the analog world and the digital systems, is used. The comparator forms the main heart of any ADC architecture used in contemporary technology for conversion from analog to digital and vice-versa. The accuracy of such converters has strong relation on design of inter stage gain amplifier and comparator.

The performance of a comparator will determine overall performance of A /D Converter because of large number of comparators is used compared to inter stage gain amplifier. The large number of comparator makes it the most critical block of a ADC architecture, not allowing efficient background calibration of all the comparators which directly affects the effective resolution of the ADC due to the comparator input offset voltage.

The overall performance of ADC the speed and the power consumption of the comparator have significant effect; owing to the enormous number of comparisons in ADC [2]. The speed of the ADC is

prime concern for high speed digital system and speed of comparator is the key factor. [3]. The prerequisite to extend the battery life of the digital system, speed and accuracy of the ADC is major concern; for comparator low offset, high speed with low power consumption is desirable. In recent years the emphasis has been given towards the design of high speed comparator with power optimization. The accuracy of the comparators confines due to offset voltage because of mismatch in V_{th}, β, parasitic and output load capacitance [8-10]. The comparator circuits should be immune to speed, power and offset trade off.

Several approaches have been proposed in the literature discussed either differential architecture or double tail architecture with offset voltage varies from 10mV to 50mV. In comparators, a lower offset comes at the cost of bigger transistor dimension therefore it will lead to more power dissipation and increased in delay. In addition, the traditional comparators are difficult to design and there are not many design procedures to lower the offset voltage. To decrease the power utilization and the area of comparators, dynamic comparators are proposed [3-6]. However, such comparators generally experience comparatively large offset voltage in comparison to static comparators [6,7]. Some designs have been proposed for dynamic comparators in the literatures. The dynamic comparators are categorized in to three groups: Resistor divider [6], Differential pair and Charge Sharing dynamic comparator [6]. Other structures are mainly derived from these architectures [3–8].

The designs proposed in literature, some are concerned with speed [7], few give emphasis to power optimization and high resolution [2], some on offset cancellation [6]. In this paper authors come out with novel design one with low offset with optimum power dissipation.

In order to break the deadlock between offset and power consumption authors have proposed novel architecture which combines the features of differential pair and double tail. The proposed architecture is more robust against any misalignment and non idealities. More importantly, it involves a significantly smaller input offset voltage without a significant rise in power and delay.

With two additional transistors inserted between output and input of the conventional dynamic comparator and converting into fully differential double tail dynamic comparator, which shows low propagation delay, with low offset voltage without any offset calibration techniques which requires more number of devices and calibration time more power hungry design strategies with optimum power and higher clock rate with the similar area, was implemented.

The paper is organized in 5 sections; Section 2 discussed the existing architecture of Differential Dynamic Comparator (DDC). Section 3 presents the novel architecture of Fully Differential Double Tail Dynamic Comparator (FDDTDC). Section 4 discussed the simulation results, section 5 concludes the paper.

1.1 Existing Architectures of Differential Dynamic Comparator

The existing Differential Dynamic Comparator (DDC) architecture is illustrated in Fig. 1[7]. When Φ_{clk} goes high comparator makes the decision. For the tail clock signal, a same phase controlled voltage swing clock has been used rather using same clock which swing from V_{SS} to V_{DD}. To ensure tail current remains in the saturation the limited clock swing is used for tail transistor M_5 and make sure that tail current not enter into linear region.

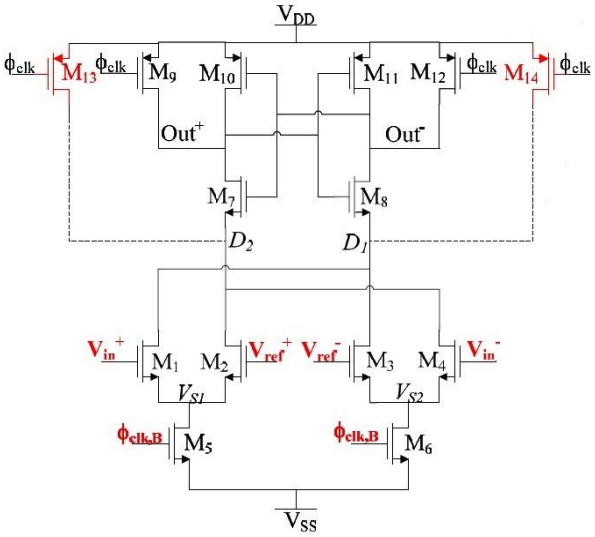


Figure 1. Differential Dynamic Comparator (DDC).[7]

All the input transistors are of the equal dimension and no imbalance is present and to ensure all input transistors M_1 to M_4 have same currents the differential pair Vin+ and Vref+ (and Vin- and Vref-) are combined in single differential pair[4,5]. During the time of decision all input transistors will contribute respectively.

The internal nodes are reset to V_{DD} when comparator is in ideal mode and help comparator to retune all the nodes prior to the comparator enters into the evaluation mode.

II. Proposed Comparator

The Fully Differential Double Tail Dynamic Comparator (FDDTDC) is shown in Fig. 2. Some modification has been made to the structure in comparison to the structure shown in Fig. 1. Transistors M_{13} and M_{14} are removed from the structure because transistors M_A and M_B will serve the same purpose to reset the internal nodes D_1 and D_2. On the removal of two clock driven transistors M_{13} and M_{14} the power dissipation of the comparator has drastically reduced in comparison to DDC. The FDDTDC can work at lower supply voltages as compared to DDC due to less stacking.

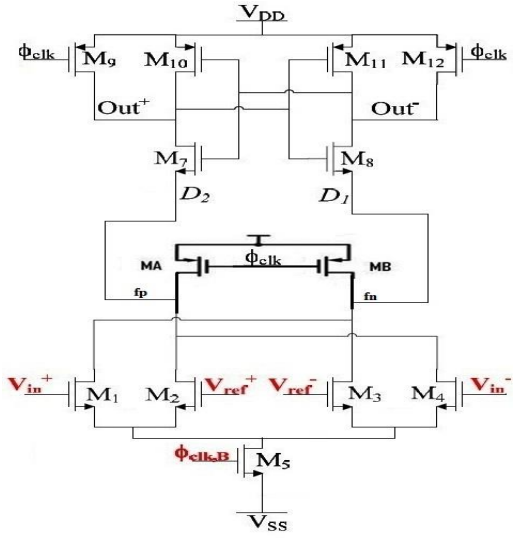


Figure 2. Fully Differential Double Tail Dynamic Comparator (FDDTDC).

2.1 Operation of the Proposed Comparator

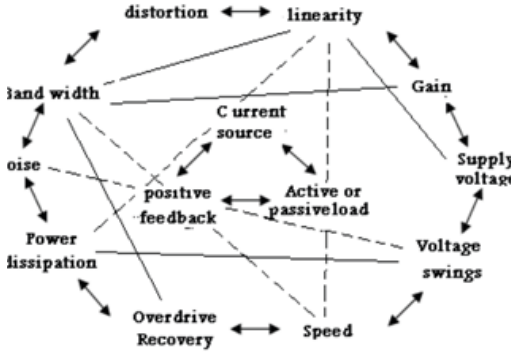
Reset Mode: When Φ_{Clk} is low, transistors M_A, M_B, M_9 and M_{12} are on. Out^+ and Out^- are precharge to V_{DD} similarly internal nodes D_1 and D_2 are retune to V_{DD}. Comparison Mode: When Φ_{Clk} is high $\Phi_{Clk,B}$ is active, transistors M_A, M_B, M_9 and M_{12} are off. Out^+ and Out^- are discharge to ground through M_1 - M_4.

The voltage at V_{in^+} is higher than the voltage at V_{in^-}, Out^- is discharged faster than Out^+. Addition of two transistors of the M_A and M_B convert the single tail comparator into double tail comparator with differential input and on removal of transistors M_{13} and M_{14} reduced the power dissipation and reduces the offset voltage and propagation delay.

2.2 Performance Analysis and Design Trade-Offs

The comparator depends on many aspects of the performance parameter. The parameters such as gain, bandwidth, distortion, voltage swings, offset, linearity, overdrive recovery and supply voltage are important along with speed and power dissipation,

and. In practice, comparator design is a multi-dimensional optimization problem because most of these constraints deal with each other. This trade-off presents many challenges in the design of high performance comparator to arrive at an optimum or compromise solution requires intuition and experience [18].



2.2.1 Offset Analysis

By definition, the offset voltage V_{OS} of the comparator equals to the differential input voltage that establishes the condition $V_{out^+} = V_{out^-}$.

In the beginning of the decision moment, M_1 to M_4 and M_5 are in the saturation region. This is the main reason of the low sensitivity of this topology to the transistor mismatch as will be demonstrate hereafter. If all the transistors of the two differential pairs have the same dimensions, $\beta_1=\beta_2=\beta_3=\beta_4$, then in the balanced point the two output currents are equal [8-9].

$$I_O^+ = I_{D7}\,, \qquad I_O^- = I_{D8}, \qquad I_{D7} = I_{D8}, \quad I_{D7} = M_2 + M_4\,,\ I_{D8} = M_1 + M_3 \tag{1}$$

$$I_{ds1} = \mu_1 C_{ox} \cdot \left(\frac{W_1}{L_1}\right) \cdot \left(V_{in+} + \Delta V_{in} - V_{t1} - \frac{V_{ds1}}{2}\right) \cdot V_{ds1} \tag{2}$$

$$I_{ds2} = \mu_2 C_{ox} \cdot \left(\frac{W_2}{L_2}\right) \cdot \left(V_{ref+} - V_{t2} - \frac{V_{ds1}}{2}\right) \cdot V_{ds1} \tag{3}$$

$$I_{ds3} = \mu_3 C_{ox} \cdot \left(\frac{W_3}{L_3}\right) \cdot \left(V_{ref-} - V_{t3} - \frac{V_{ds3}}{2}\right) \cdot V_{ds3} \tag{4}$$

$$I_{ds4} = \mu_4 C_{ox} \cdot \left(\frac{W_4}{L_4}\right) \cdot \left(V_{in-} - V_{t4} - \frac{V_{ds3}}{2}\right) \cdot V_{ds3} \tag{5}$$

$$I_{ds7} = \mu_7 C_{ox} \cdot \left(\frac{W_7}{L_7}\right) \cdot (V_{out+} - V_{s7} - V_{t7})^2 \tag{6}$$

$$I_{ds8} = \mu_8 C_{ox} \cdot \left(\frac{W_8}{L_8}\right) \cdot (V_{out-} - V_{s8} - V_{t8})^2 \tag{7}$$

The threshold voltage V_{th} and μC_{ox} can be explicit in terms of a nominal part and a deviation part owing to mismatch between M_7 and M_8. For ease of calculation collective deviation between μ and C_{ox} can be consider as only deviation in mobility μ. [8-9].

$$\mu_7 = \mu_n + \Delta\mu_7 \tag{8}$$

$$\mu_8 = \mu_n + \Delta\mu_8 \tag{9}$$

$$V_{t7} = V_{tn} + \Delta V_{t7} \tag{10}$$

$$V_{t8} = V_{tn} + \Delta V_{t8} \tag{11}$$

The random mismatch in the threshold and mobility of transistor pair can be modeled as follows [8-9]:

$$\sigma_{V_{th}}^2 = \frac{A_{V_{th}}^2}{WL} + S_{V_{T0}}^2 D^2 \tag{12}$$

$$\sigma_{\mu}^2 = \frac{A_{\mu}^2}{WL} + S_{\mu}^2 D^2 \tag{13}$$

Where A_{Vth} is process-dependent parameter, S_{VT0} is the variation of V_{T0}, W, L are the width and length of transistor pair, D is the distance between the

transistor pair in layout. In 180nm CMOS process, for nMOS is $A_{Vth} \approx 5mV \cdot \mu m, A_{\mu} \approx 1.04\ \%$. For pMOS $A_{Vth} \approx 5.49mV \cdot \mu m, A_{\mu} \approx 0.99\ \%$.

The mismatch between M_2 and M_3 random offset is:

$$\sigma^2_{V_{OS\_M2M3}} = \sigma^2_{V_{t2}} + \sigma^2_{V_{t3}} + \left(V_{ref+} - V_{d5} - V_{tn} - \frac{V_{ds2}}{2}\right)^2 \cdot \sigma^2_{\mu_2/\mu_n} + \left(V_{ref-} - V_{d5} - V_{tn} - \frac{V_{ds3}}{2}\right)^2 \cdot \sigma^2_{\mu_3/\mu_n} \quad (14)$$

The mismatch between M_1 and M_4 results in random offset is

$$\sigma^2_{V_{OS\_M1M4}} = \sigma^2_{V_{t1}} + \sigma^2_{V_{t4}} + \left(V_{in+} - V_{d5} - V_{tn} - \frac{V_{ds1}}{2}\right)^2 \cdot \sigma^2_{\mu_1/\mu_n} + \left(V_{in-} - V_{d5} - V_{tn} - \frac{V_{ds4}}{2}\right)^2 \cdot \sigma^2_{\mu_4/\mu_n} \quad (15)$$

The mismatch between M_7 and M_8 results in random offset is

$$\sigma^2_{V_{OS\_M7M8}} = \left(\frac{W_8}{W_1}\right)^2 \frac{(V_{out-} - V_{s8} - V_{tn})^2}{V^2_{ds1}} \sigma^2_{V_{t8}} + \left(\frac{W_7}{W_1}\right)^2 \frac{(V_{out+} - V_{s7} - V_{tn})^2}{V^2_{ds1}} \sigma^2_{V_{t7}} + \left(\frac{W_8}{W_1}\right)^2 \frac{(V_{out-} - V_{s8} - V_{tn})^4}{4 \cdot V^2_{ds1}} \sigma^2_{\mu_8/\mu_n} + \left(\frac{W_7}{W_1}\right)^2 \frac{(V_{out+} - V_{s7} - V_{tn})^4}{4 \cdot V^2_{ds1}} \sigma^2_{\mu_7/\mu_n} \quad (16)$$

The mismatch between M_{10} and M_{11} results in random offset is

$$\sigma^2_{V_{OS\_M10M11}} = \left(\frac{W_{10}}{W_1}\right)^2 \frac{(V_{DD} - V_{out+} - V_{tn})^2}{4 \cdot V^2_{ds1}} \sigma^2_{V_{t10}} + \left(\frac{W_{11}}{W_1}\right)^2 \frac{(V_{DD} - V_{out-} - V_{tn})^2}{4 \cdot V^2_{ds1}} \sigma^2_{V_{t11}} + \left(\frac{W_{10}}{W_1}\right)^2 \frac{(V_{DD} - V_{out+} - V_{tn})^4}{16 \cdot V^2_{ds1}} \sigma^2_{\mu_{10}/\mu_n} + \left(\frac{W_{11}}{W_1}\right)^2 \frac{(V_{DD} - V_{out-} - V_{tn})^4}{16 \cdot V^2_{ds1}} \sigma^2_{\mu_{11}/\mu_n} \quad (17)$$

In general static random offset voltage σ_{Vos} in the proposed Fully Differential Double Tail Dynamic Comparator is as follows:

$$\sigma^2_{V_{OS}} = \left(\sigma^2_{V_{OS\_M1M4}} + \sigma^2_{V_{OS\_M2M3}} + \sigma^2_{V_{OS\_M7M8}} + \sigma^2_{V_{OS\_M10M11}}\right)^{1/2} \quad (18)$$

For Differential Dynamic Comparator static random offset voltage σ_{Vos} is as follows:

$$\sigma^2_{V_{OS}} = \left(\sigma^2_{V_{OS\_M5M6}} + \sigma^2_{V_{OS\_M1M4}} + \sigma^2_{V_{OS\_M2M3}} + \sigma^2_{V_{OS\_M7M8}} + \sigma^2_{V_{OS\_M10M11}}\right)^{1/2} \quad (19)$$

2.2.2 Delay Analysis

The delay is characterized as the time between the start of the amplification phase and the time where 50% of the latch final output is reached. Based on this definition, the inner latch delay can be calculated from derivations presented in [16-17].

The delay of the comparator consists of two key parts, t_0 and t_{latch} [13].

Delay of Differential Dynamic Comparator (DDC) as follow:

$$t_{delay} = t_0 + t_{latch} \quad (20)$$

$$t_{delay} = 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2,3,4}}}\right) \quad (21)$$

$$t_{delay} = 2\frac{C_L|V_{thp}|}{I_{M5}+I_{M6}} + \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{M5}+I_{M6}}{\beta_{1,2,3,4}}}\right) \quad (22)$$

Delay of FDDTDC as follow:

$$t_{delay} = t_0 + t_{latch} = 2\frac{V_{Thn}C_{Lout}}{I_{M5}+I_{M6}} + \frac{C_{Lout}}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \quad (23)$$

$$t_{delay} = 2\frac{V_{Thn}C_{Lout}}{I_{M5}+I_{M6}} + \frac{C_{Lout}}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}\cdot I_{M5}^2\cdot C_{L,fn(p)}}{8V_{Thn}^2 C_{Lout} g_{m1,2,3,4}\,\Delta V_{in}}\right) \quad (24)$$

2.2.3 Power Analysis

In dynamic comparator power is expressed as below [21].

$$P_{avg} = f_{clk}V_{DD}I_{sp5}\left(\frac{1}{8n\emptyset_t^2}\right) \cdot \tau_{latch}|V_{Thp}| \times \left[2k - n|V_{Thp}| + (2k + n|V_{Thp}|) \cdot exp\left(-2\frac{t_p - t_0}{\tau_{latch}}\right) - 4K \cdot exp\left(-\frac{t_p - t_0}{\tau_{latch}}\right)\right] \quad (25)$$

In the equation, k is equal to the V_{DD}-$|V_{Thp}|$ and t_p and t_0 are

$$t_0 = \frac{C_{Load}|V_{Thp}|}{I_{tail}/2} \quad (26)$$

$$I_{tail} = I_{M5} + I_{M6} \quad (27)$$

$$t_p = \frac{C_{Load}}{G_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{\Delta V_{in}}\right) \quad (28)$$

Equation (25) indicates that the dominant design parameters are clock frequency, size of input transistors, V_{DD} and evaluation period (t_p-t_0) which influence the most on the power consumption of the comparator.

III. Simulation Result

To verify its operation and the consistency with the analytical derivations including delay, offset ICMR, frequency response and input –output noise spectral density. The circuit operates from a ± 0.9V power supply. The simulation results shown in Fig. -4 to 18, the delay of FDDTDC comparator is 0.37ns, offset voltage is 0.36mV, ICMR is -0.40 V to 0.56V with power consumption of 216.37mW which is quite low in comparison Differential Dynamic Comparator. The FDDTDC can successfully resolve difference of 1mV (10 bit resolution for $1V_{p\text{-}p}$ input swing) at 1.3GS/S. Considering that there is no extra circuitry require for offset cancellation, the new-flanged design is appropriate for applications demanding high resolution, high speed with optimum power.

2.3Simulation Results of DDC

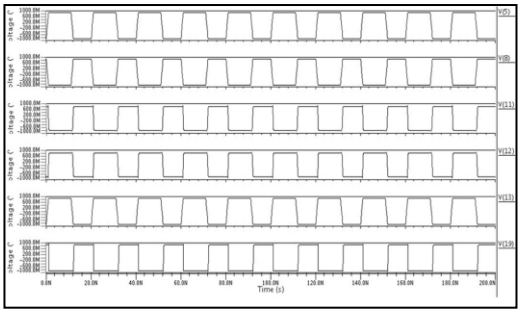


Figure 4. Transient Analysis of DDC.

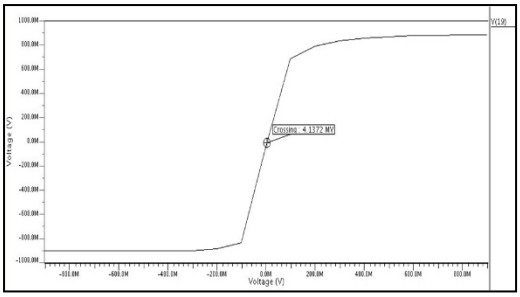


Figure 5. Offset Voltage of DDC.

2.4 Simulation Results of FDDTDC

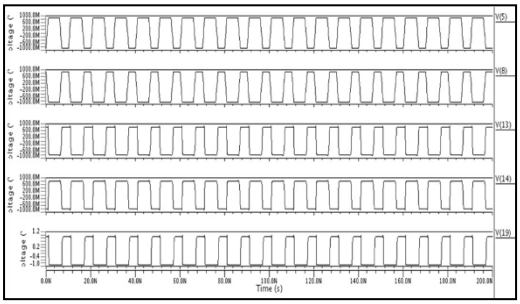


Figure 10. Transient Analysis of FDDTDC.

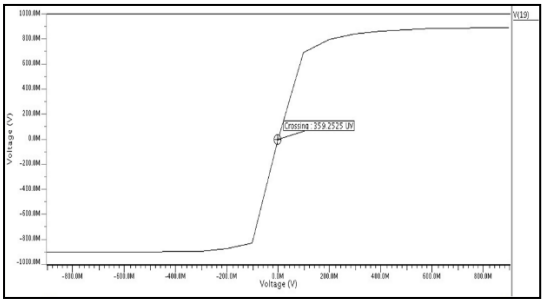


Figure 11. Offset Voltage of FDDTDC.

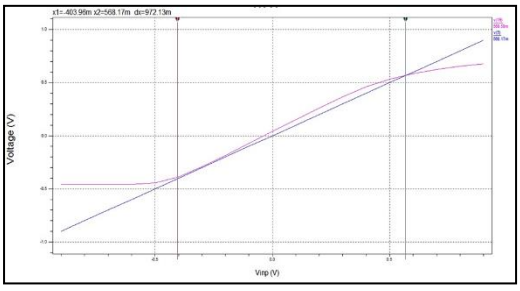


Figure 12. ICMR of FDDTDC.

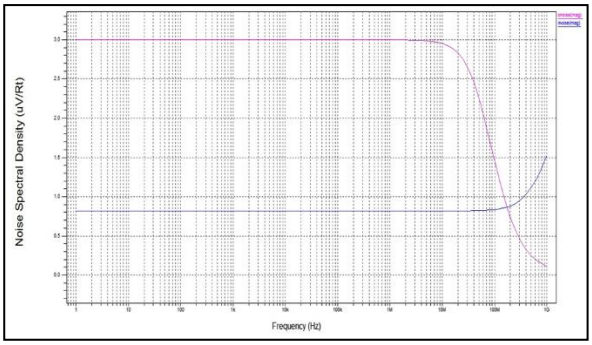


Figure 13. Input-Output Noise Spectral Density of FDDTDC

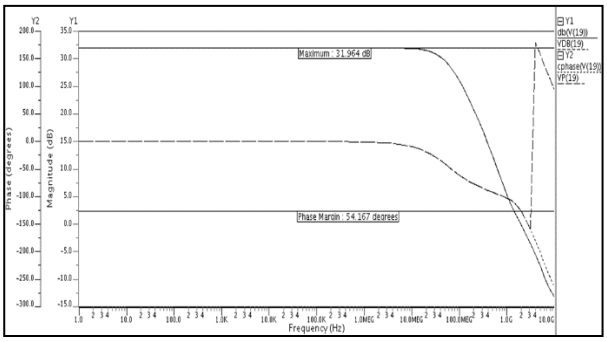


Figure 14. Frequency Response FDDTDC.

Fig.-9 and 15 shows comparator layouts. Particular care was taken in the layout to avoid mismatch to avoid affecting delay and power of the comparator.

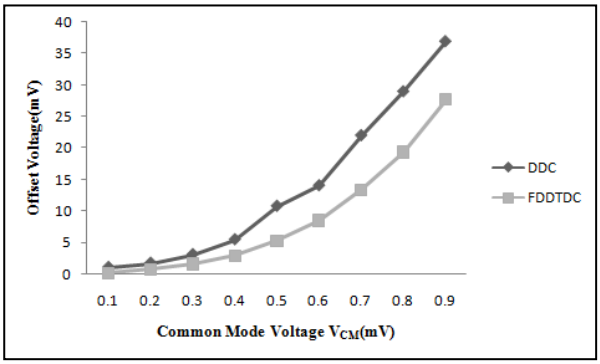


Figure 16. Common Mode Voltage v/s Offset Voltage.

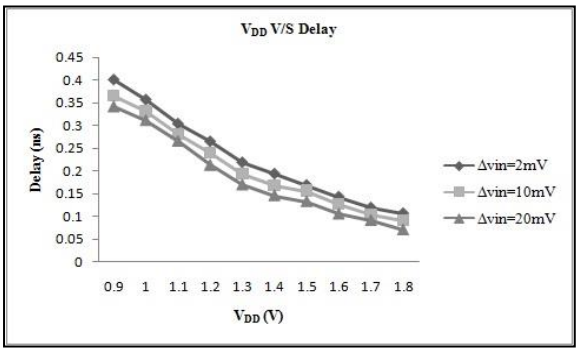


Figure 17. Delay v/s Supply Voltage.

Fig.-16 illustrates the sensitivity of the input referred offset to input common mode voltage (V_{CM}). The Proposed Fully Differential Double Tail Dynamic Comparator has low offset voltage as compared to DDC mentioned in the Fig. 1.

Fig.-17 demonstrates the simulation results of the delay of FDDTDC versus variation in supply voltage. The delay of the FDDTDC is significantly reduced with higher differential input voltage.

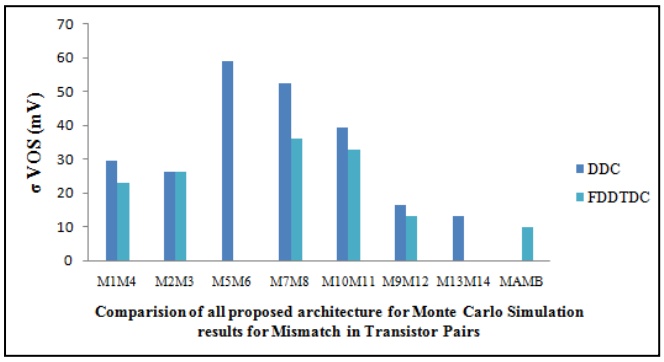


Figure 18. Mismatch Analysis.

Figure 18 illustrates the mismatch analysis between transistor pairs and effects of offset voltage due to individual pairs as mentioned in equation (18) and (19).

Table 1 evaluates the performance of the FDDTDC with the DDC. The overall noise spectral density at the input is similar in the case of DDC and DDTDC. The FDDTDC comparator provides the high gain, low offset, with high dynamic range with better sensitivity at low input with power optimization with considerable reduction in delay.

As Table 2 shows, the FDDTDC has the very low offset and lowest FOM energy dissipated per conversation for optimum power.

Table 1: Performance Comparison

Parameter	DDC[7]	FDDTDC
Technology (nm)	*180 nm*	
Supply Voltage (V)	*±0.9*	
No. of Transistors	*14*	*13*
Sampling Frequency	*250 MS/s*	*1.3GS/s*
Delay (ns)	*0.680*	*0.37*
Offset(mV)	*4.1*	*0.36*
ICMR(V)	*-0.30 to 0.49*	*-0.40 to 0.56*
Gain (dB)	*29.261*	*31.964*
PSRR⁺(dB)	*67.18*	*72.00*
PSRR⁻(dB)	*57.72*	*64.48*
CMRR(dB)	*64.88*	*82.93*
Noise Spectral Density (μV/√Hz) @ input-Output	*0.91 & 3.64*	*0.81 & 3.00*
Sensitivity (mV)	*4*	*1*
Bit Resolution	*8*	*10*
Power Dissipation (μW)	*379.82*	*265.25*
PDP (fJ)	*15.69*	*8.59*
FOM (fJ/decision)	*5.93*	*0.20*
Area (μm x μm)	*16.5 x 17.6*	*15.03 x 17.09*

Table 2: Performance Summary and Comparison

Reference	[10-12]	[13]	[14]	This Work
Technology (nm)	*90*	*180*	*90*	*180*
Supply Voltage (V)	*1*	*1.2*	*1.0*	*±0.9*
Sampling Frequency(GS/s)	*3.0*	*0.5*	*1*	*1.3*
Delay (ns)	*0.17*	*0.29*	*0.15*	*0.37*
Resolution (bits)	--	--	--	*10*
Offset(mV)	*16.3*	*7.8*	*33*	*0.36*
Power(μW)	*162*	*329*	*51*	*265.25*
PDP (fJ)	--	--	--	*8.59*
FOM (fJ/decision)	*59.20*	*658*	*51*	*0.20*

IV. CONCLUSION

A novel design structure of Fully Differential Double Tail Dynamic Comparator for high performance ADC is proposed with comprehensive offset analysis and expressions is derived. The simulation results illustrates that a comparator designed with the proposed techniques is 45% faster, and 30% more power efficient. The FDDTDC exhibits 91% low offset without any power hungry offset cancellation circuits as compared with conventional comparator. The FDDTDC makes a superior trade-offs among speed, resolution, power, offset and area.

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