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Rapid Multiplier Architecture for Area and Power Optimization

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ABSTRACT

The interest in unique devices has increased with the special development of low power, digital signal processing (DSP) systems used in mobile computers and portable multimedia applications. Multipliers plays a major role including its DSP program. Operator duplication is often used not only on DSP chips but also on many public key cryptosystems such as Elliptic Curve Cryptography (ECC) and RSA. The proposed 4-bit Vedic multiplier's performance is analysed in terms of average power dissipation, delay, and also scaling effect of supply voltage.

Keywords : Public-key cryptosystems, Elliptic Curve Cryptography (ECC) and RSA.

I. INTRODUCTION

The multiplier plays an important role in electronic systems where repetition can be used in Digital Signal Processing applications such as convolution and fft. There is therefore a need for high speed and dynamic dynamics on a daily basis.

In the current case there are various types of repetition available such as Array Multiplier, Wallace Tree Multiplier Dock Repeat, but retrieval of members similar to the Wallace tree multiplier will simply increase the positive numbers, so that overcoming this duplicate of booths is built but duplicate booth applies to smaller designs.

The Vedic extension has been introduced to resolve the redundacy. Vedic repetition will increase both positive as well as negative numbers. The strength and delay of multiplication are increased and decreased respectively using Gate Diffusion Input (GDI) techniques.

Sri Bharati Krishna Tirtha Maharaja introduced the calculation of Vedic figures from the Vedas known as the Indian Sanskrit during the period 1911-1918. Vedic Mathematics relies on 16 sutras, numerical operations, arithmetic and dynamic arithmetic. The most widely used sutra is Urdhva Tiryagbhyam which provides a successful restoration. Decreased power consumption in integrated circuits has used a variety of methods. The GDI cycle has been used to reduce energy consumption and acceleration [2]. Standard CMOS circuit and GDI Mux based circuit breaker circuit and related investigations. In 2 X 2 Repetition of Vedas AND door and expansion of large parts are outstanding.

II. METHODS AND MATERIALS

A. Vedic Mathematics:

Vedic-arithmetic is an exceptionally old framework that can be applied legitimately to different parts of science, for example, variable based maths, math, and so forth. It eliminates vulnerability by eliminating superfluous strides before estimating any outcomes. There are 16 sutras in Vedic-arithmetic Urdhva Tiryakbhyam (UT) and Nikhilam Navatashcaramam Dashatah (NND) used to quantify the augmentation of any two numbers. Normally, the NND sutra is favored by huge pieces and UT sutra is favored by littler numbers. The UT sutra is consequently utilized in this work.

B. Urdhva Tiryakbhyam (UT):

Urdhva Tiryakbhyam (UT) means "vertical and transverse" operation which will multiply two numbers with any basis. The two 3-bit numbers, say U [2:0] and V[2:0] are multiplied to obtain a carry denoted by C[3:0] and Y[2:0] denotes partial production of the commodity. Then the following steps need to be taken:

Step1: C0Y0 = U0V0
Step2: C1Y1 = {(U0*V1) + (U1*V0)} + C0
Step3: C2Y2 = {(U0*V2) + (U1*V1) + (U2*V0)}+ C1
Step4: C3Y3 = {(U1*V2) + (U2*V1)} + C2
step5: C4Y4 = {(U2*V2)} + C3
Hence, the final product = C4Y4Y3Y2Y1Y0

C. Two Bit Vedic Multiplier:

This method is described below in two numbers, 2-input bits of 'A' and 'B' where A = a_1a_0 and B = b_1b_0. Next, the less important pieces' increase, which gives very little noticeable end product (vertical). Then the multiplicand LSB is multiplied by the next high multiplication value and added by the LSB multiplication product and the next higher multiplicand fraction (crosswise). The sum provides a second item of the final product and the carrying is added to the partial product obtained by multiplying the bits that are most important to provide the quantity and handling.

The sum amount is the corresponding third indicator and the bearing is one-fourth of the final product. The 2X2 Vedic multiplication module is operated using four inputs AND gates and two additions. It is found that the construction of Vedic 2x2 hardware is similar to traditional Array Multi 2x2 bit architecture. It is therefore assumed that the repetition of 2-bit binary numbers in the Vedic method did not have a significant impact on the development of the multiplication efficiency. Specifically, the total delay is only 2-half of the add-on delay after the production of the final products, which is very close to the Array duplicate. Thus, a 4x4 bit Vedic multiplier using a 2x2 bit multiplier turns into a building block. The same method can be changed for 4 & 8 input pieces. But with the highest number of input bits, a small change is required.

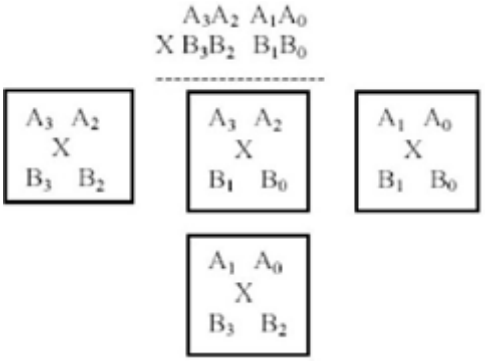

Figure 1 Sample Presentation for 4x4 bit Vedic Multiplication

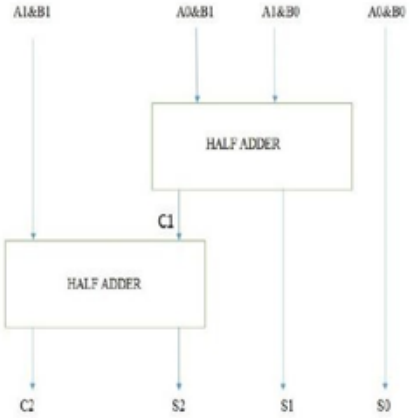

Figure 2 2-bit Multiplier with HA's

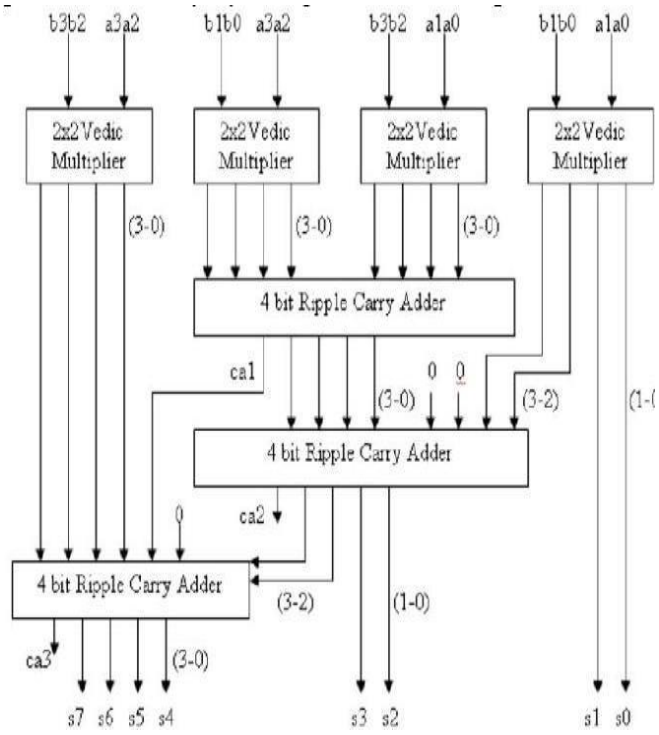

Figure 3 Schematic of 4x4 bit Vedic Multiplier

Fig .3 represents a Vedic multiplication module for implementing 4x4 multiplication. This is realized with the help of four-2x2 bit Vedic multiplier modules. To test 4x4 multiplication, taking into account, A = A3 A2 A1 A0 and B = B3 B2 B1 B0, the output line of the output result would be "S7S6S5S4S3S2S1S0", such that 'A' and 'B' are broken into two categories. It states A3A2 & A1 A0 from 'A' and B3 B2 and B1B0 from 'B'. Using the Veda multiplication base, take two pieces at a time and use a 2-bit repetition block.

Each block square appeared is a 2x2 bit multiplier. The primary 2x2-bit inputs are A1A0 and B1B0. The last square block is marginally duplicated by 2x2 with the addition of A3 A2 and B3 B2 Medium shows two 2x2 piece products by embeddings A3 A2 and B1B0 and A1A0 and B3 B2.

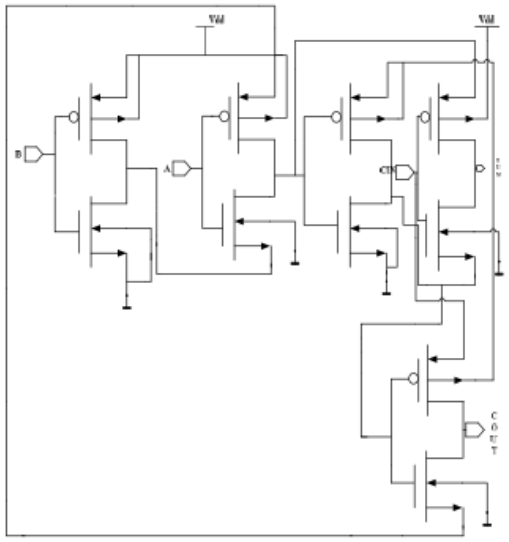

Figure 4 Schematic Full Adder circuit

A schematic of the 4x4 bit Vedic multiplier is shown in Fig. 4. For the final product "S7S6S5S4S3S2S1S0", four-2x2 multipliers of with a 4-bit Ripple-Carry Adders (RCA) are offered. The proposed Vedic multiplication can be used to reduce delays. Early writings refer to the Vedic repetition based on many repetitive structures. On the other hand, a new phase-specific construction is proposed here.

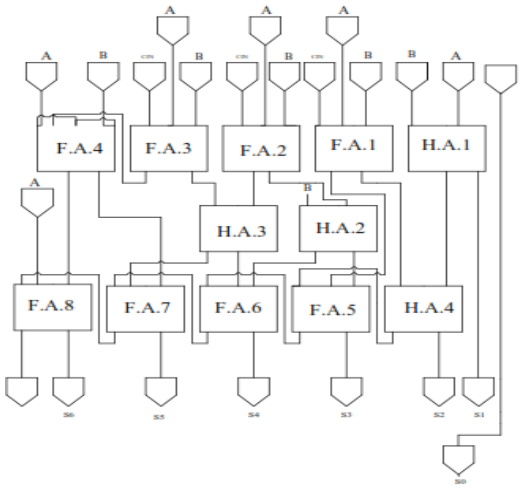

Figure 5 Proposed 4x4 Vedic Multiplier

The arrangements for RC Adders are shown in Fig. 5, effectively reduces the delay. Interestingly, the Vedic 8x8 multiplication modules are well utilized using four 4x4 multiplication modules. That is why GDI based add-on and full adder are used to perform 4-bit Vedic calculations.

III. RESULTS AND DISCUSSIONS

The Proposed methodology is implemented as half adders and full adders using TENSOR flow IDE. The compressor schematic diagrams are represented in Fig.6.

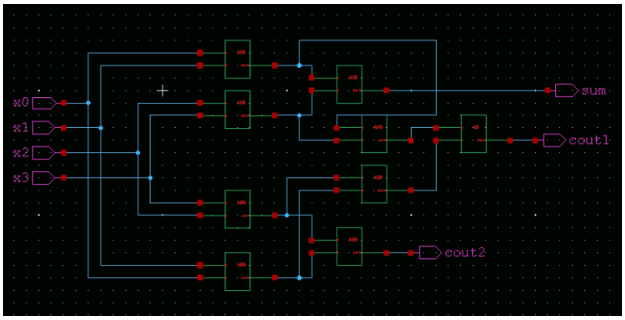

Figure 6 Compressor Schematic

The full adder schematic is represented in Fig.7 and the simulated output for the proposed 4x4 Vedic multiplier is represented in Fig.8.

GDI circuit result for full and a half full the adder is represented and includes the product of the power delay, Table 1.

Table 1 Basic Blocks Comparison

Block	Power Dissipation (In W)	Delay (In Nano Sec)	Power Delay Product (In Joules)
Conventional			
Half Adder using GDI logic	18.07p	15.51	0.136f
Conventional Full Adder	21.45p	69.87	0.0116f
Full Adder Using GDI Logic	46.71p	30.26	0.002f

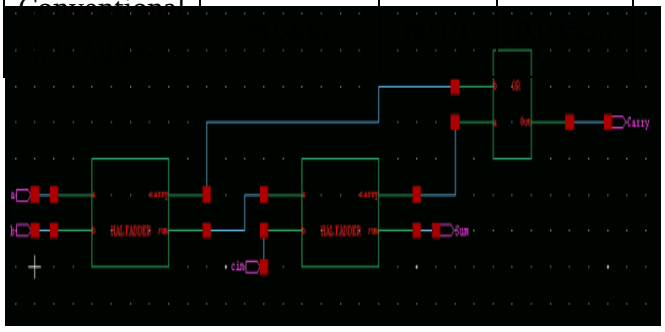

Figure 7 Full Adder Block Representation.

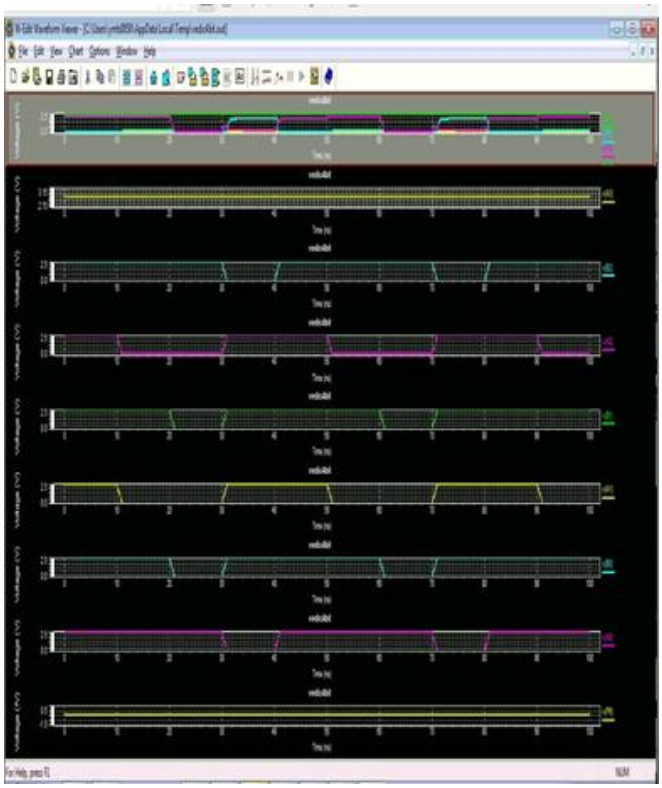

Figure 8 Simulation Results of 4x4 Vedic Multiplier

GDI-powered add-on power reduced to 18.07pW, and for full installation using GDI reduction is 46.71pW.

Table 2 4x4 Vedic Multiplier

4x4 Vedic Multiplier	Power Dissipation (In W)	Delay (In Nano Sec)	Power Delay Product (In Joules)
With Conventional CMOS	13.0574u	0.93	12.14f

With GDI Technique	39.109p	0.929	0.036z

Delays are also reduced in comparison CMOS circuits. Table 2 gives the power distribution and distribution 4x4 Vedic multiplication delay using standard CMOS and GDI circuits.

IV. CONCLUSION

In this paper, a method of rapid multiplication based on ancient Indian Vedic mathematics is proposed. It is a generic method based on the N-bit Vedic multiplier that would be used for digital signal processing. The proposed 4-bit Vedic multiplier is compared to the traditional multiplier, andd the Vedic multiplier has better efficiency. The proposed multiplier provides higher output for higher order bit multiplication. Thus, the results of the present study indicated that the Vedic multiplier is an effective multiplier and useful for digital signal processing applications.

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