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Receiver Designs for Electronic Toll Collection Systems : A Survey

Rarika Ravi, Anu Assis
Electronics and Communication, TKM College of Engineering, Kollam, Kerala, India

ABSTRACT

This paper discusses about different receiver designs adopted so far for various electronic toll collection systems. A comparative analysis based on the discussions is also provided. It shows that each design has it's own advantages and disadvantages compared to others. The main aim of this paper is to identify the most suitable design. The researches shows that the receiver design described in the 5.8GHz digitally controlled DSRC receiver for Chinese electronic toll collection system is the most suitable one. Here all RF, IF blocks and digital baseband for on-chip automatic gain control, are integrated on an RF-SoC. The proposed digitally controlled LNA and mixer circuits are elaborated. The technology used is 0.13μm CMOS technology. The RF block occupies a chip area of 0.75mm2. It consumes 22mA under a 1.5V supply voltage. The bit error rate maintains better than 10-6, the input power level varies from -75dBm to -8dBm. This design provides a receiver sensitivity improvement of at least 25%, and a dynamic range enhancement of at least 12%.

Keywords : DSRC 5.8 GHz receiver, Electronic toll collection systems, On-chip AGC, Intelligent transportation system (ITS), X/Ku-band, LNA.

I. INTRODUCTION

Electronic toll collection systems are commonly used for vehicular communication / smart transportation. ETC aims to eliminate delay on toll road, toll bridge, toll tunnel etc. It provides an efficient radio communication link between an on-board unit (OBU) and a roadside units (RSUs). ETC system makes this possible by using Dedicated Short Range Communication Channel. DSRC system using 5.8GHz ISM band is widely used. DSRC systems are globally expanding their applications to the vehicle-to-vehicle and the vehicle-to-infrastructure communication for safety and information exchange [1].

Most of the currently distributed DSRC systems are implemented as hybrid compartments which have several chipset parts and lots of external components [1]. In order to satisfy the specific requirements of a system, many of currently providing hybrid modules should be returned to the laboratory for replacement or manual calibration of related components.

The DSRC system consists of a transmitter an receiver module commonly known as DSRC system transceiver. The receiver architecture is very important for efficient communication. There are certain challenges involved in the design of a receiver for DSRC system.

The challenges are low cost, low power, small size, high sensitivity, wide dynamic range and low bit error rate. In most of the designs the receiver is made up of an RF block and an IF block, where the RF block consists of low noise amplifier (LNA), mixer and local oscillator (LO) and the IF block consists of band pass filter (BPF), power gain amplifier (PGA), analog to digital converter (ADC) and received signal strength indicator (RSSI).

This survey deals with different works published so far on DSRC receiver designs. It mainly concentrates on receiver designs , modifications and outcomes. A comparative analysis is also presented.

II. LITERATURE SURVEY

Sangho Shin et al., [1] proposes a receiver architecture based on three significant features

i) TDD switch and the frequency synthesizer should have very fast switching transient speeds when a radio switches between RX- and TX-modes.

ii) The TX should deliver the output power of +10dBm with regulated tolerance of less than ±0.5dB, since the communication zone is critically defined.
Additional temperature compensation circuitry is definitely needed to stabilize the output power throughout the wide temperature range.
iii) The sensitivity power of a RX circuit must be controlled with fine accuracy covering wider than 36dB control range from 76dBm to -40dBm.

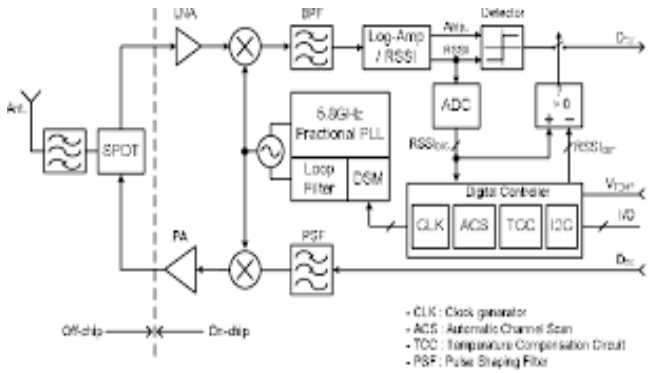

Fig 1: Block diagram of 5.8GHz DSRC chipset [1]

Low IF architecture is chosen to build the receiver for its superior noise and offset performances over the zero IF ones. Since it is low IF, the hardware complexity is low and thus consumes low power. But it takes too long to sense RSSI and the image rejection become problematic. The sensitivity is set at a level higher than the minimum receiver sensitivity of ITS, the receiver noise figure doesn't increase from the best noise figure since the gain and noise budget will not be changed. The proposed method is very easy to compensate the temperature effects by simply updating the RSSIset with respect to the sensed temperature.

In Jeongki Choi et al., [2] by using a wake-up radio receiver (WuRx) architecture the power dissipation is minimized and sensitivity is maximized. WuRx are designed by a simple RF envelop detector consisting of Schottky diodes or MOSFETs. It doesn't use active filters and amplifiers for input signal amplification. The only thing need to be considered is the performance of RF envelop detector (RFED). The system uses a low power, high gain RFED and a low power delay based BPF (DBPF) that has a narrow and sharp frequency response that sufficiently rejects interference.

The WuRx consists of an RFED, a comparator and a DBPF. The receiver is similar to WuRx except for the implementation of the front-end LNA to increase sensitivity. The input ports of the WuRx and Rx shares the same antenna. A external 1:N balun transformer is used to maximize the gain of the RFED at a given current consumption. A switching power amplifier based polar transmitter is used. The down link signal of the Chinese ETCS consist of a wake-up pattern and a normal pattern.

The WuRx should provide an interrupt signal to modem part in response to the wake-up pattern to enable the Rx to receive the normal frame. Extra AM interferences are removed by DBPF. Therefore DBPF reduces the probability of false wake-up significantly. The paper Xiaofeng He et al., [3] presents the design of a 14mW receiver without phase locked loop (PLL) for Chinese ETC system. The primary goal is low power consumption. The Chinese standard requires the system to be battery powered not vehicle

powered. A low power receiver has been presented in a 0.13um CMOS process. For balancing power consumption and sensitivity a PLL less receiver architecture is considered.

Comparing the power consumption of 10.8mW with the power consumption of other designs in which a PLL is included shows a power saving of at least 50%. Both the RF front end and PLL take a large portion of the overall consumed power in the low-power and low-data low-IF receiver.

The sensitivity of the receiver is the higher the better with a fixed amount of power consumption. Sensitivity of -70dBm is targeted. To achieve this the noise figure (NF) of the receiver must be less than 19 dB. Two amplification stages are utilized at the RF front end. two amplification stages are utilized at the RF front end. One is a fixed-gain low-noise amplifier (LNA), and the other is an active balun with variable-gain functionality. An RF power detector (RFPD) replaced a down-conversion mixer, the received signal strength indicator (RSSI) and the peak holder operate together with the data slicers to demodulate the received ASK signal. RSSI is required to dynamically control the gain of the receiver, thus the bit error rate (BER) will not deteriorate. This has automatic gain control (AGC). A 4-bit digital control voltage, i.e., VC_Digital , is generated to control the gain of the active balun. The LNA has a fixed gain of 20 dB. A cascode LNA is adopted at the first stage, which is designed to have a fixed gain of 20 dB.

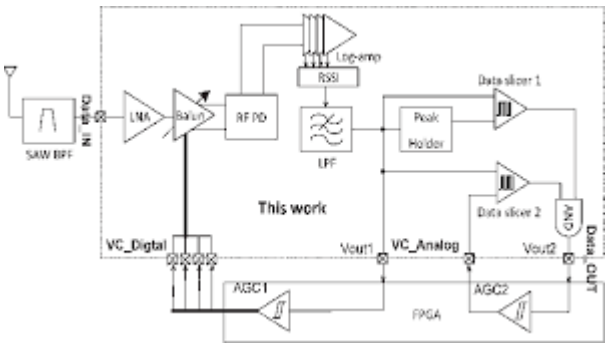

Fig 2: Block diagram of the proposed system approach [3]

The source inductor Ls is implemented by several parallel-connected bond wires, whereas the gate inductor is implemented by an off chip inductor. In the second stage, two common-source (CS) amplifiers are used to form a balun, such that differential signals are generated. The balun also acts similar to a variable-gain amplifier.

In the third stage, a cross-coupled capacitor common-gate amplifier is utilized to enhance without consuming any extra power. In this PLL and a down-conversion mixer are absent and the frequency down-conversion is performed by the RFPD.

In Kuduck Kwon et al., [4] the receiver uses low-IF conversion architecture for high sensitivity and low-power consumption while the transmitter uses direct up-conversion architecture for its simple structure and reliability. The RF front-end of the integrated 5.8 GHz DSRC transceiver is implemented using 0.13 m CMOS technology, the overall noise figure of the receiver is less than 5 dB whereas image rejection ratio of more than 30 dB, and the transmitter carries an output peak power of 10dBm with the adjacent channel power ratio of 43 dBc. The CMOS RF front-end of the 5.8 GHz integrated DSRC transceiver for the Korea/Japan ETCS is presented. The transceiver is highly integrated and satisfies all specifications, without an external low-noise amplifier (LNA), an external channel filter, and an external PA.

A Low-IF receiver selects the proper IF which has no image signal in image band and adopts single-quadrature architecture with a proposed transconductor-type quadrature generator in RF signal path to solve image problem for both Korean and Japanese ETCSs. In the ETCS, the receiver dynamic range must be controlled to communicate properly in designated toll area. The accurate sensitivity control is required because the receiver sensitivity defines the toll area spatially. That is, when the sensitivity is lower than the desired level,

the OBE will start communication before it enters the toll area and thus, it can interrupt the other DSRC devices. In the opposite case, the available time for the communication will be insufficient. The zoned communication also regulates the transmitter output power of the OBE. In Korea/Japan ETCS, the transmitter should deliver the output power of 10 dBm with regulated tolerance of less than 1.0 dB throughout the in-vehicle temperature variation from to 85.

A low-IF architecture is chosen over the zero-IF one for the receiver due to its superior noise and dc offset performances. The low-IF receiver can also be implemented with much lower hardware complexity than a high-performance heterodyne receiver, thereby consuming less power. However, the image rejection should be required to solve image problem in the low-IF receiver. The choice of IF is important since it is strongly related with the image rejection, received signal strength indicator (RSSI) settling time, and the design complexity of IF circuits such as the BPF and RSSI/Log-Amp circuits.

The paper by Jeongki Choi et al., [5] deals with a fully integrated 5.8 GHz DSRC short range communication transceiver with a 10uA interference aware wake-up receiver (WuRx) that operate with a low standby and operating current consumption. A high-gain RF envelope detector using a voltage-boosting method is proposed for both the WuRx and receiver (Rx) to reduce the current consumption. The high-power ASK modulator used extends output dynamic range with low power consumption.

Additionally, a delay-based bandpass filter is adopted in the WuRx to filter out interference from automotive applications, thus increasing the battery life time by reducing the probability of a false wake-up. For battery powered OBU, in Chinese ETCS, a wake-up receiver is mandated. Therefore the DSRC transceiver presented in the authors' prior work [4] cannot be used in the Chinese OBU due to the absence of a WuRx and because of its high current dissipation of approximately 150 mA, although it has excellent performance.

The transceiver is a fully integrated low-current CMOS transceiver with a WuRx that satisfies all specifications of the Chinese ETCS. In the proposed transceiver, a high-gain RFED is proposed for the signal-to-noise ratio (SNR) improvement in both WuRx and Rx while the proposed high-power ASK modulator saves power consumption in the transmitter (Tx). It is done without a loss of dynamic range. The envelop detector increases the gain by approximately $4N^2$ times compared to that of the conventional topology. It uses a low-power delay-based bandpass filter (DBPF) as a substitute for the conventional RC filter in the WuRx. This leads to the sharp interference filtering without external surface acoustic wave (SAW) filters. In order to increase sensitivity a two-stage differential LNA with LC-tuned loads is used and it is placed in front of the RFED.

Hyunwon Moon et al., [6] proposes a low noise and low power RF front-end for 5.8 GHz DSRC (Dedicated Short Range Communication) receiver. The RF front-end consist of a single-to-differential two-stage LNA along with a Gilbert down-conversion mixer. A single-to-differential LNA with capacitive cross coupled pair is used, which removes an external balun and 5.8 GHz LC load tuning circuit. A differential LNA is preferred in RF SoC (system on a chip) but this needs passive baluns to convert single-ended signal to differential signal. It adopts the CS amplifier with CGCS balun as the single-to-differential-converter.

To obtain low NF and high gain, the LNA consists of the single-to-differential converter and a differential capacitive cross-coupled cascode amplifier. The LC tuning is required for high gain so switched capacitor array is used for variable capacitance. The low noise amplifier includes variable gain function.

In Masashi Yamagata et al., [7] proposes a 7 to 15 GHz low noise amplifier for wireless communication receiver. It is a differential X/Ku-band LNA is a two-stage fully differential common source design. A differential design reduces the sensitivity to common mode parasitics such as ground and supply wire-bonds at the expense of a larger chip area. Due to the large size of required on-chip transmission lines at these frequencies , on-chip spiral inductors and metal-insulator-metal (MIM) capacitor are used throughout the design.

Lingling Cao et al., [8] proposes a 5.8GHz digitally controlled DSRC receiver for Chinese electronic toll collection system. All RF, IF blocks and digital baseband for on-chip automatic gain control, are integrated on an RF-SoC. The proposed digitally controlled LNA and mixer circuits are elaborated.

The main contribution of this work is a digitally controlled receiver architecture is, where the gain of RF front end is directly controlled by the AGC algorithm running in the digital baseband. All RF, IF and baseband circuits are integrated as an RF-SoC to minimize the system size and cost.

When the receiver is activated , RF signal from the antenna is amplified by LNA. Then with the help of local oscillator signal from the PLL, the mixer converts the 5,8 GHz RF signal down to 5MHz IF signal. The output signal from the mixer and programmable gain amplifier are sampled by an RSSI circuit and digitized by ADCs. Based on this signal, an AGC algorithm sends proper digital control signals to adjust the gain of LNA, mixer and PGAs and to maintain an appropriate signal magnitude into the main ADC.

TABLE I. COMPARATIVE ANALYSIS

Table-1 Comparative Analysis

Reference	[1]	[2]	[3]	[4]	[5]	[8]
Technology	0.18µm CMOS	0.13µm CMOS	0.18µm CMOS	0.13µm CMOS	0.13µm CMOS	0.13µm CMOS
Rx structure	With PLL	PLL-less	PLL-less	With PLL	With PLL	With PLL
Frequency	5.8 GHz	5.8 GHz	5.8 GHz	5.8 GHz	5.8 GHz	5.8 GHz
Sensitivity	-76 dBm	-61 dBm	-50 dBm	-84 dBm	-61 dBm	-75 dBm
BER	N/A	N/A	10^{-6}	10^{-5}	N/A	10^{-6}
Return loss	N/A	N/A	-24 dB	-14 dB	N/A	<-23.7 dB
Noise Figure	<17 dB	N/A	<19 dB	5 dB	<19 dB	<15 dB

III. CONCLUSION

i) The use of a mixer in the proposed architecture [8] leads to certain chip area and power overhead.
ii) The drawbacks of low gain, poor BER, high output noise and degraded sensitivity resultant
from the use of envelope or power detector [3]-[5] are eliminated.
iii) The designs in [2]-[5] require off-chip devices, such as transformer or FPGA. This has increased the system size. The design [8] is fully integrated for minimum system size and cost.
iv) In contrast with analog control, digital control has potential to realize higher accuracy via sophisticated algorithms.
v) The area of digital baseband will shrink with technology scaling. It is flexible and convenient
for designers. Therefore, the proposed digitally controlled receiver architecture is inherently compatible with the AGC algorithm.

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