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Design and Implementation of Programmable Analog Board

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ABSTRACT

Prototyping of analog circuits is hair stretching work, and often get's complicated because one has to work with breadboard. To eliminate bread boarding of big digital systems, FPGAs were developed over the past years for prototyping purposes. We have come up with similar thing for analog world. It's like FPGA, but instead of digital it will create analog circuits like integrator, differentiator, adder based on coding. We have one plan to make it possible. FPGAs use RTL coding like VHDL/verilog and has their own s/w which converts coding to circuit net list and which gets implemented in FPGAs, now at this stage we don't have that much knowledge to develop our own synthesizer s/w, hence we'll use following plan. We will have OP-AMPs in circuit, and passive components which has capability to change it's value based on programming. For resisters we use something known as digital POTs and for capacitors NCD2100 which is digital programmable variable capacitor. We'll have interconnection between all of them via FETs, which will act as programmable switches. Now for programming, one has to write commands, which will be decoded by ASCII codes and accordingly switch matrix is programmed to form desired circuit. There is digital circuit which accepts ASCII bits and programs solid state switches, and with this one can implement amps, integrator, differentiators, adders, instrument amplifiers and combination of all above. Application of this thing can be found in prototyping, educational purposes and implementation of PID controllers.

Keywords: RTL coding, VHDL, Design Analysis, ASCII codes, capacitors NCD2100, PID controllers, FPGA

I. INTRODUCTION

Electronic switching is the basic requirement to achieve programmability in circuit synthesis, instead of fixed connection, we need variable connection between electronic components. Prototyping of analog circuits is hair stretching work, and often get's complicated because one has to work with breadboard. To eliminate bread boarding of big digital systems ,FPGAs were developed over the past years for

prototyping purposes. We have come up with similar thing for analog world. It's like FPGA, but instead of digital it will create analog circuits like integrator, differentiator, adder based on coding. We have one plan to make it possible. FPGAs use RTL coding like VHDL/verilog and has their own s/w which converts coding to circuit net list and which gets implemented in FPGAs, now at this stage we don't have that much knowledge to develop our own synthesizer s/w, hence we'll use following plan. We will have OP-AMPs in circuit, and passive components which has capability to change it's value based on programming. For resisters we use something known as digital POTs and for capacitors NCD2100 which is digital programmable variable capacitor. We'll have interconnection between all of them via FETs, which will act as programmable switches. Now for programming, one has to write commands, which will be decoded by ASCII codes and accordingly switch matrix is programmed to form desire circuit. There is digital circuit which accepts ASCII bits and programs solid state switches. And with this one can able to implement amps, ntegrators, differentiators, adders, instrument amplifiers and combination of all above. Application of this thing can be found in prototyping , educational purposes and implementation of PID controllers.

Edmund Pierzchala,Milwaukie,Marek A. Perkowski proposed, There is disclosed a programmable analog or mixed analog/ digital circuit. More particularly, this invention provides a circuit architecture that is flexible for a programmable electronic hardware device or for an analog circuit whose input and output Signals are analog or multi-valued in nature, and primarily continuous in time. There is further disclosed a design for a current-mode integrator and Sampleand-hold circuit, based upon Miller effect. This patent has same application as we thought,but it does not include any OPAMP based circuits.Plus it doesn't mention anything about the way of programming it.

Dean R. D'Mello , P.Glenn Gulak elaborate, The drive towards shorter design cycles for analog integrated circuits has given impetus to several developments in the area of Field-Programmable Analog Arrays (FPAAs). Various approaches have been taken in implementing structural and parametric programmability of analog circuits. Recent extensions of this work have married FPAAs to their digital counterparts (FPGAs) along with data conversion interfaces, to form Field Programmable Mixed-Signal Arrays (FPMAs). This survey paper reviews work to date in the area of programmable analog and mixed-signal circuits. The body of work reviewed includes university and industrial research, commercial products and patents. A time-line of important achievements in the area is drawn, the status of various activities is summarized, and some directions for future research are suggested.

Khaled A. El-Ayat proposed model state that, A user programmable IC contains user programmable analog portion, a user programmable digital portion and one interface portion which contains ADC and DAC, and one user configurable interconnect portion. This Mixed signal IC is amalgamation of FPGA and FPAA. It's slightly different from our pure analog configurable circuit board. Otherwise the way of realizing programmability in interconnect is same as we are planning. There is no discussion on programming method as well.

Jianhua Yang, Muhammad Shakeel Qureshi, Gilberto Medeiros Reibeiro,R. stanley Williams,developed a model This paper A field-programmable analog array (FPAA) includes a digital signal routing network, an analog signal routing network, Switch elements to interconnect the digital signal routing network with the analog signal routing network, and a configurable analog block (CAB) connected to the analog signal routing network and having a programmable resistor array. The Switch elements are implemented via digital memristors, the programmable resistor array is

implemented via analog memristors, and/or antifuses within one or more of the digital signal routing network and the analog signal routing network are implemented via digital memristors. This is work is same as what we want to do.It includes CAB(Configurable analog blocks),which has resistor and capacitor banks which is used to achieve desired value of respective parameter. Switching network for programmable interconnection between CABs. This paper displays total hardware information .It proposes the use of 'Memristor' to eliminate low speed isolated gate transistors, which is used as switch. Most of the configurable passive elements available with few op-amps. This paper has much in-depth technical information compare to our level.

James L. Gorecki,Bill G. Gazeley,Yaohua Yang proposed it as immediate to conclude that A double differential comparator can be efficiently implemented utilizing a first comparator Stage having a folded cascode with floating gate input terminals and clamped Single-ended output, and a capacity coupled input stage for transferring a weighted Sum of input Signals to the floating gates of the first comparator Stage. Additionally, the differential comparator can be integrated into fully differential programmable analog integrated circuits. Such fully differential programmable analog integrated circuits can also include a differential output digital-to-analog converter to be used with or without the double differential comparator. This paper is different then our product. Authors discussed mainly comparators circuits and programmability in the same. There were no use of OP-AMPs.

T S Hall, G D Gray, P Hasler build a theoretical proposal While their specific architectures vary, their small sizes and often restrictive interconnect designs leave current FPAAs limited in functionality and flexibility. For FPAAs to enter the realm of large-scale reconfigurable devices such as modern field-programmable gate arrays (FPGAs), new technologies must be explored to provide area-efficient accurately programmable analog circuitry that can be easily integrated into a larger digital/mixed-signal system. Recent advances in the area of floating-gate transistors have led to a core technology that exhibits many of these qualities, and current research promises a digitally controllable analog technology that can be directly mated to commercial FPGAs. By leveraging these advances, a new generation of FPAAs is introduced in this paper that will dramatically advance the current state of the art in terms of size, functionality, and flexibility. FPAAs have been fabricated using floating-gate transistors as the sole programmable element, and the results of characterization and system-level experiments on the most recent FPAA are shown.

Tyson S., David V Anderson proposed a model Floating-gate analog circuits are being used to implement advanced signal processing functions and are very useful for processing analog signals prior to analog to digital conversion. We present an architecture analogous to FPGA architectures for rapid prototyping of analog signal processing systems. These systems go beyond simple programmable amplifiers and filters to include programmable and adaptive filters, multipliers, gains, winner-take-all circuits, and matrix-array signal operations. We discuss architecture as well as details such as switching characteristics and interfacing to digital circuits or FPGAs.

Based on this literature review, it can be concluded that analog programmable array has a great effectiveness for upcoming use. A comprehensive research has been performed to select different material, method and designing of different safety system that offer features such as productivity,eco friendly, economical produced base in a large scale and benefit for users. Conceptual task has been performed on the provision of programming system and theoretical expressions introduced, based on ideal

assumptions. The proposed technique figured out new factors for design of an effective safety system. The Knowledge with respect to the factors governing for safety system is beneficial for the society and accordingly, suitable modifications are introduced into the proposed model. Their effects on the using and efficiency are plotted for the proposed system.

DESCRIPTION OF WORKING PROCESS

Those who have used FPGAs might know it about it's working. First there goes a software/compiler which allows you to write command which implements the functionality you want. They also allows you to simulate your designs before you synthesize it.VHDL/verilog codes then converted into opcodes that goes into your FPGA board,where it has LUT(Look-up table) and cross-bar switches to have interconnect between them, with which your circuits gets synthesized. Our Prog-Analog board will work exactly same way. Where we have an 8-bit processor which will do the job of compiler, it decodes the incoming commands. Based on inputted command, processor will make/brake switches in cross-matrix switch IC 2 and programs the inputted/calculated value for passive parameters(Resistors and Capacitors) in programmable POTs and CAPs.

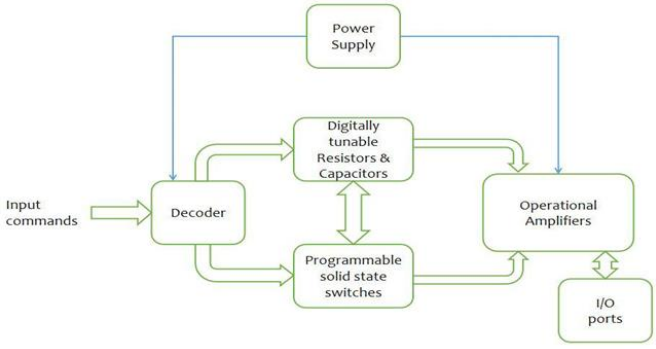


Figure 1. Block diagram Working operation

The block diagram is pretty self explanatory. Operational amplifiers are the key components in almost all analog designs. It has bank of OP-AMPs and digitally tunable POTs and CAPs in input of the OP-AMP as well as in feedback. Digitally tunable POTs and CAPs has fixed inbuilt resisters and capacitor banks with switching transistors and decoding/interfacing logic all built upon a silicon wafer inside DIP/SOP form-factor. Programmable solid state switches is crossbar switch matrix which is the heart of Telecomm switching systems. It has cross-point FET switches with decoding/interfacing logic circuit inbuilt in DIP/QFP/PLCC form-factor. However such things are made for low power applications and often has low bandwidth problem and cross-talk problem.

II. METHODS AND MATERIALS

Hardware Part:

Cross-Matrix switch IC

Programmable XMatrix switch is the heart of our project. It comes with programmable inter-connect solid state switches w/ programming, decoding, level shifting circuits.

We are using IC CD22M3494 from Renesas Electronics. It's a 16 x 2 (128 total switches) bidirectional cross-matrix switch IC.

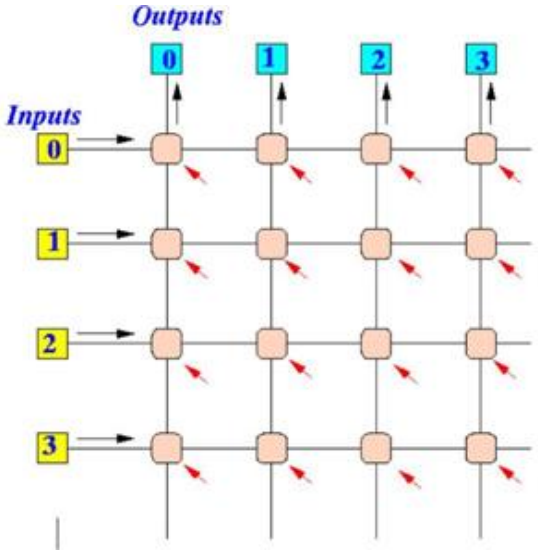


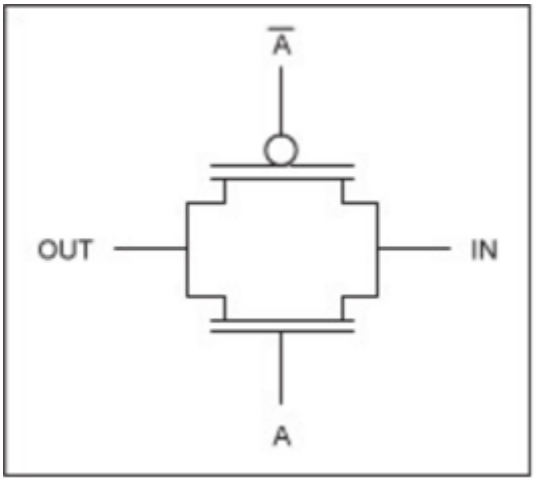
Figure 2. Cross-bar switch

Each of skin like coloured box is a transmission gate. It's a bidirectional FET switch controlled by logic '1' or '0'.

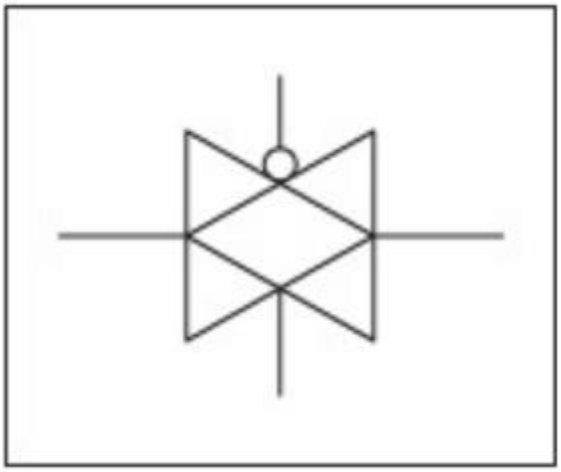
When TG(Transmission gate) at 00 intersection is closed,Input0 is connected to output0.
When all TGs along Input0 is closed,In0 is connected to all 4 outputs.
When TGs at 00 and 10 is connected, then in0 and in1 is connected to each other as well.

Transmission Gate:

A transmission gate is a electronic device, which either blocks or passes signal from input to output based on status of control signal. It's often called 'Analog switch'.



(a) Schematic



(b) Symbol

Figure 3. Transmission gate circuit and symbol

It consist of P-channel and N-channel MOSFETs in parallel, thus allowing bi-directional current low. It permits signal to swing up-to the supply rails .Beside the 2 MOSFETs ,there are additional logic circuit to make it a fully functional switch.

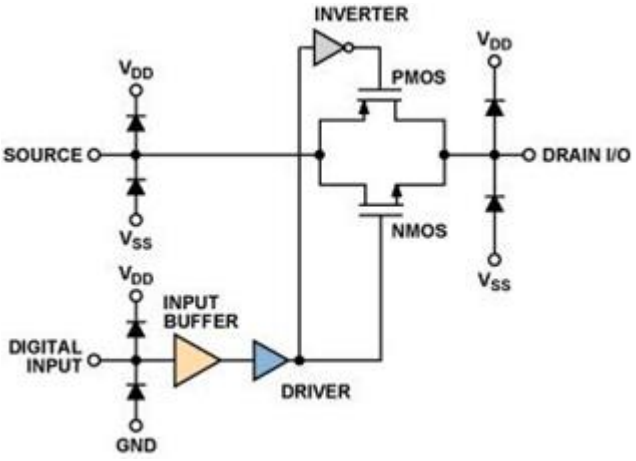


Figure 4. Analog switch circuitry

Diodes at the input and output terminals are for ESD protection. Now we know that the negative VGS will break the channel in NMOS and positive VGS will break channel in PMOS.

When positive voltage (VDD) is applied at the digital input, it turns ON the NMOS and complementary negative rail from inverter will turn ON the PMOS. Now as Drain voltage approaches the gate voltage, channel begins to pinch from the drain side also known as saturation. But here is the catch, when one MOS is having it's channel pinching o ,other MOS starting to having it's channel coming out of pinch-ing and since both MOS are in parallel, it's like having 2 resistors in parallel, when one of is increasing resistance, other is decreasing hence parallel combination maintains equivalent resistance of TG fairly constant for the signal swinging upto the rails as shown in plot of resistance below

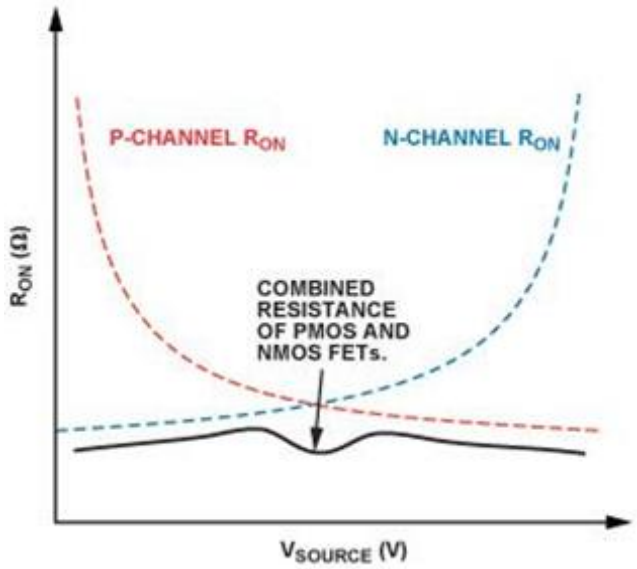


Figure 5: Analog switch RON plot

Above discussion just the use of TG instead of using single MOS.As in absence of body diode,a MOS can act as bidirectional switch but to have optimum performance with rail to rail swinging,we need TG.

More about CD22M3494

CD22M3494 is an array of 128 switches arranged in 16x8.Meaning it has 16 horizontal lines and 8 vertical lines with each intersection containing one TG.Below the block diagram of CD22M3494...

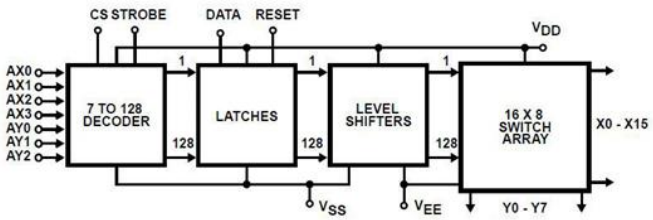


Figure 6 : CD22M3494 block diagram

Now let's discuss each block one by one. At the front end we got 7 to 128 decoder which points to any one out of 128 TGs, as on 7-bit code on input. It has directly 7 bit data lines, some other commercial products do come with SPI,I2C blocks as a front end! Which occupies lesser pins of your microprocessor. The 7 bit code determines that ON or OFF command has to be given to which TG.

Latches block contains D-latches. This acts as a memory block which contains the record of ON and OFF of all 128 TGs. Data has to be written here only once .Note that it's a volatile memory and has a power on reset function, meaning in power on condition, all the TGs will be OFF by default.

RESET pin is active HIGH RESET. Upon triggered it resets outputs of the D latches to '0'.DATA pins is used to determine any TG(pointed by 7-bit code to the decoder) to ON or OFF. Writing '0' on Latches will turn OFF TG, while writing '1' on latches will turn ON TG.STROBE pin provides the clock for the latches, which are negative edge triggered.

Level shifter converts unipolar digital signal to bipolar control signal for all TGs. As input signal is swinging up to the rails. Using unipolar digital to the gates of TGs will leads you to the inappropriate results. Consider depletion type PMOS for example, if we apply logic '0' to it's gate to turn it ON, but input signal is swinging up to the rails, so when Vs is negative ,it makes VGS positive and reduces the conductivity of the channel. Hence if we want signal to be passed nicely with rail to rail swing then we need to convert logic levels VDD and 'DGND' to VDD and VEE. Such cross, metrics switch ICs are mixed signal ICs, meaning it has digital and analog portions. So we need different 'DGND' and 'AGND'. Level shifter block does the job of isolating DGND from AGND.

And the last switch array block contains all TGs and 16X8 IOs.Level shifter output is given to Gates of the FETs.

Electrical parameters of CD22M3494

Table 1: Electrical parameters of CD22M3494

Max DC supply voltage VDD w.r.t VEE	16 Volts
Max DC Transmission Gate current	25 mA
Typical ON resistance rON	36-40
Leakage current IL	10 A
-3 dB frequency response	50 MHz
Cross talk @ 1 MHz	-30 dBV(As per our own measurement)

ATmega64A Microcontroller:

ATmega64A is an 8-bit microcontroller from AVR(Advanced Virtual RISC) family by ATMEL. It's the brain for our Prog-Analog board. The number 64 in it indicates that it has 64 Kbyte of ash(code) memory. This is the bridge between programmer and the board. It communicates with the computer via USB, with software called 'Tera Term'.It's a terminal software and it is the place where programming code will be written. Microcontroller will receive this codes and decode(comparing it with pre-stored and identify that which one is entered!) it,then it does 2 things,(1)make/brake switches in Xmatrix switch IC and (2)Programs the given/computed resistance values to the digital trim POT X9C103.

ATmega64 is doing the job of an interpreter. One by one it decodes and exe-cutes instructions written by the programmer. It also does the job of checking of any harmful connection for example, say you made direct connection between OP-AMP's output to the inverting input. Now if some reason if you connect inverting pin of OP-AMP to the ground then it'll short output of OP-AMP to the ground and that can damage the OP-AMP or may be it pass the current way higher then XMatrix switch IC's capabilities, thus by damaging it. All this will be done by ware that will goes inside the chip.

Controller also points out all kinds of error that it can identify, like invalid instruction, connection error, etc. It has 2 LEDs on board on is green(for OK) and other is red(for ERROR).They will have certain blinking pattern based on which error can be displayed or it can be shown on the terminal software Tera Term.

ATmega64A is clocked from 16 MHz crystal oscillator. It's capable up to 20 MHz. Below are some features of the ATmega64A

Table 2: ATmega64A Features

Operating voltage	2.7 - 5.5 Volts
Brown out detector	YES
Flash size	64 Kbyte
Watchdog timer	Available
Pin count	64
Packages	DIP,QFP,QFN
EEPROM size	2 Kbytes
USART	2
General purpose registers	32
PWM channels	8
SRAM size	2 Kbytes

OP07C

OP07C is another very important component. It's a precision operational amplifier from Texas Instruments. Below are the list of features it has...
Low noise
Low input o set voltage(60 V) Wide supply range(18 Volts)
ESD rating(HBM/CDM) up to 1000 Volts
Differential voltage gain(at specialized conditions) 400 V/mV GBP of 600 KHz
slew rate is 0.3 V/ s CMRR of -120 dBV
Input resistance ri is about 33 M

OP07Cx is precision OP-AMP. Meaning it has very low inherent noise, low parameters drift, low quiescent current. All of our circuit that can be synthesized on, will contain a OP-AMP. We are using 3 OP07C OP-AMPs in our design. We got one OP-AMP and digital POTs(X9C103), xed capacitors, XMatrix switch build around it as a one block. We have such 3 blocks on our board.

Each block's output can be fed directly to any other block including the block it-self. Thus allowing cascading of the blocks. Allows to implement n-order. For example each block can synthesize 1st order butterworth lter, then all blocks can be cascaded by providing output from each block to the input of next block and we can synthesize 3rd order butterworth lter. Now any block can get input from any other block e.g. feedback from 3rd block to 1st block. Thus allowing to synthesize more complex circuits like bi-quad lters like circuits.OP07C's input o set voltage is not that impressive but it does come with o set null pins. We have trim pot connected with null pins hence you can reduce the o set voltage by adjusting it.

Digital potentiometer - X9C103:

Digital POT is another very important component in our project. It allows to synthesize the resistance of whatever value we want. Now trim pots has in nit resolution or extremely tiny step size is achievable, but the digital POT is as it name suggests is digital(discrete) and has some what bigger step size. Step size means the amount of resistance it can increase/decrease. Digital POTs are available in resistance range like 100 ,1K ,10K ,100K .Each has different step size, higher the value higher the step size. For the all resistance values shown before the step size is 1 ,10 ,100 , and 1K respectively.

X9Cxxx are the digital POTs from Inter as 8-pin IC. They are bit too costly but looking to their performance with lower parasitic, it totally worth it! All discussion above and from now are for particular X9Cxxx series digital POTs They have array of xed value resistance etched out on a silicon die along with wiper switches, control section and interface section, and small non-volatile memory.

Features of the X9C103:

Table 3: X9C103 Features

Supply voltage V_{CC}	5 Volts
Max voltage on V_H and V_L w.r.t V_{SS}	8 Volts
$V = \|V_H - V_L\|$	10 Volts
Max wiper current(I_W)	10 mA
Power rating	10 mW
Wiper resistance	40
Wiper parasitic capacitance	25 pF
Resistance variation	20 %
Temperature coefficient	300 PPM/ C

Working of the X9C103 is very simple.103 number indicates it is the 10K POT. It has a step size of 100 .Step size also referred as the resolution. Which is 1% of the POT's value. This is the amount by which resistance value is in-creased/decreased.

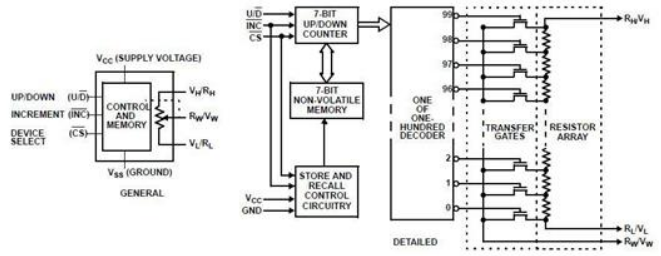


Figure 7 : X9C103 Block diagram

There are 100 resistors of about the same values are built in.Each is of value equals to the resolution(i.e 100 for the our case).Now as shown in the gure : 9 there are 100 pass transistors as well. All of which is controlled by binary to decimal decoder for 0 to 99.When for example 50th transistor is turned on, all the resistance before that will come in series and adds up their resistance. You see that it has 3 terminals VH ,VW and VL because it's a POT. There are ICs available as a digital rheostats which comes with only 2 terminals.

Now the controlling action. It has 3 pins for the controlling of the DPOT. Datasheet say it as a 3 - wire interface. Those pins are U/D, INC,CS. It has 7-bit UP/DOWN counter on chip, who's output is given to decoder which decodes 0 to 99 and resets to 0 in other cases. U/D pin decides whether to UP count or DOWN count. CS for chip select use full when we have chained the number of X9C103s like in our case.INC for the input pulse which acts as a clock input for the UP/DOWN counter. Getting to the any resistor is like getting higher gears in bike. You have to start from the lower gears. Same is the case with this, we have to start from the lower resistance and goes up to the max limit and roll o back to the lower. Lower limit is not the dead short but it's equal to wiper resistance mentioned in table 3.

It also consists a 7-bit EEPROM. Where any 7-bit code from the counter can be stored and it will be applied to decoder after POWER ON RESET as a default. By taking CS pin to HIGH while keeping the INC to HIGH will copy the content of the counter into the EEPROM.

Power supply design:

For our board we require dual rail power supply as normal OP-AMP based circuits need. We designed 5 Volt power supply, with old style linear regulator based design. We have used L7805 for +5 Volts and L7905v for -5 Volts. Each has current delivering capacity of 1.5 Amps which is way more then what we need!

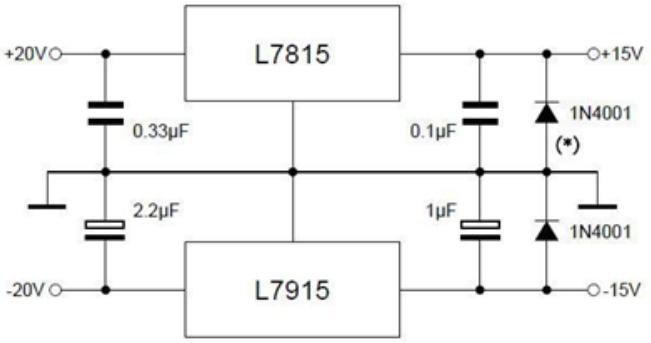


Figure 8 : Power supply circuit

One down side of the L78xx and L79xx based design is that it's high noise. Noise level is as high as 200 VRMS. Noise level is not good if we want to have some audio processing using the prog-analog board. We have used it's SMD version, the package D2PAK.The front end has step-down transformer then the FBR and then the circuit shown in the figure.

Quad SPST solid state switch - ADG202A

Initially we wanted to have NCD2100 IC, which is digital variCAP. It's design and working is pretty much same as X9C103.It has pre-built capacitors array and series pass transistors. But due to it's high cost, low capacitance value(few pico-Farads only),unavailability in Indian market, we droped it. There no other alternatives to that IC with higher capacitance value and lower cost. It seems that all

those ICs are designed to be implemented in high frequency designs up to hundreds of MHz, but our requirement is different. We have moderate frequency OP-AMPs and we have designed our board by keeping the 100 kHz limit in mind. So we decided that we will go with the xed values passive capacitors. We chose all ceramic capacitors because of it's low cost, wide range of values, small size and it's non polarized. We have used SMD(CDC and MLCC) ceramic capacitors. So we have now DPOT and xed value capacitors. But we still want some choices on the xed value capacitor so we decided to put lot o xed value capacitors with interconnect switches so that user can select between xed value capacitors. For that some of capacitors are directly connected to the XMatrics switch but there are already lot of components connected with XMatrix, so we included another small switching IC.

IC is ADG202A.It's a 4 channel, SPST solid state switch from Analog devices. We have selected it because of it's low cost and availability to the local vendor.

Table 4 : ADG202A features

Max supply voltage range	44 Volts
Signal range	15 Volts
ON resistance(R_{ON})	60
Leakage current I_L	0.5 nA
Power dissipation	33 mW
Cross talk	-80 dB
Parasitic capacitances(C_S and C_D)	5 pF

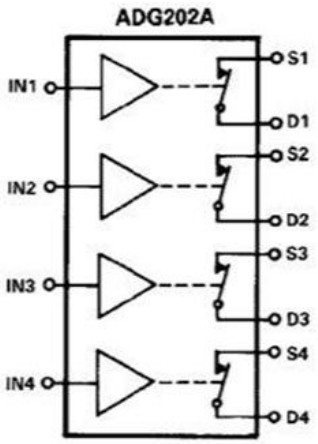


Figure 9 : ADG202A

WORKING OPERATION IN FLOW CHART (Software part)

This flowchart shows that how to operation will be done by the main program in software part. that should be accurate command and proper direction should be given for getting efficient operational output.

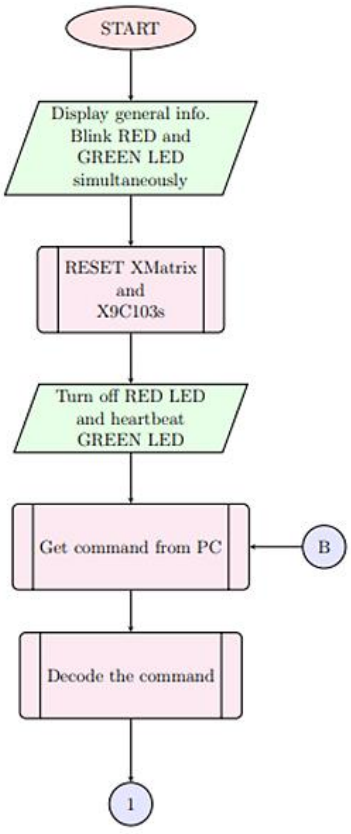


Figure 10 : Flowchart of working operation

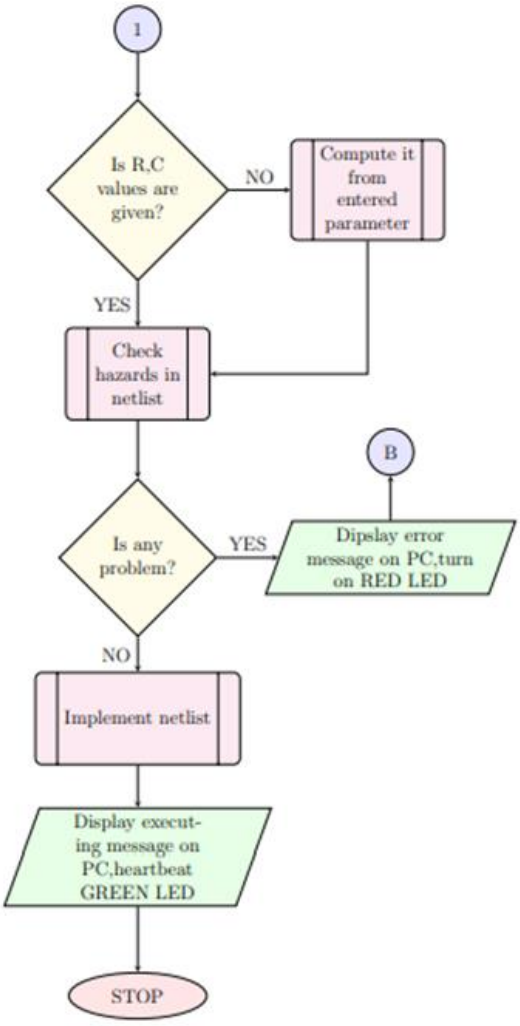


Figure 11: Flowchart of working operation

FACTOR CONSIDERATION DURING THE DESIGN

Well Maintained Environment

At the time of designing and make structural function for getting benefited outcome, well maintained environment is needed for better output of result. The system should be well maintained with sufficient effort, and all functional parts should be well sound maintained. The outcome where work will be reflected should be fulfilled all that conditions.

Good Efficiency

All that efficiency will depend upon the proper connection as well as order nomination of all parts of device that can give a good result with ensure of betterment.

Eco-Friendly

The device working process is very much eco friendly there is no collision in between components and the safe has been ensure for users.

III. RESULT AND DISCUSSION

Pictures on given below shows the virtual 3D look of our Prog-Analog board. It's a 2 layer PCB with components on both the side. Power supply on the bottom right, microcontroller with USB 2.0 support hardware on bottom left(see figure 12).In middle we have 3 CD22M3494 XMatrix switch ICs. We have 6 BNC connectors,3 for Input and 3 for Output. So it's much convenient to provide input directly from the function generator. Total 180+ components. OP-AMPs on the right portion of the board with offset trim POTs, directly connected to Output BNCs. Top left we got 2 Audio SMD female jacks for Audio input. Female header is also provided for each block for extra inputs and external components connection. Slider switch is given for setting the Input impedance to either HIGH-Z or 50 Ω.Small LED for indication of 50 Ω.At the bottom we have ERROR RED LED and GREEN OK LED.

FPAA abbreviation of Field Programmable Analog Array exists which does the job of synthesizing analog circuits. There are CAB(Configurable analog blocks) and programmable interconnects, some includes OP-AMPs as well. Such things are based on "Switched capacitor technology", which is popular because capacitor is easy to fabricate on a silicon wafer then the resistor, but it's not "truly" analog.

OUTCOME OF THE PROJECT

Hardware and Firmware design of analog development board which can allow to synthesize circuits based on programming.

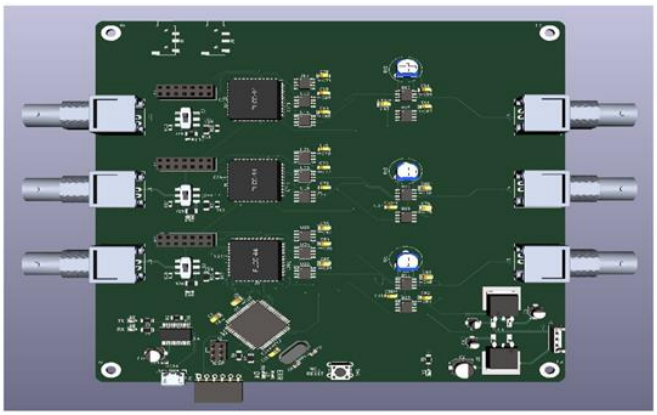


Figure 12: Virtual 3D model of Prog-Analog board

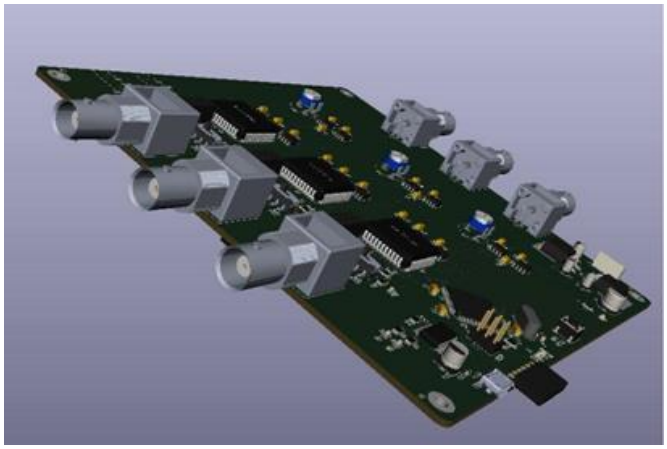


Figure 13: Side view

Here showing the virtual model of whole operational system in project work. that has given lot effort with good outcome operational review with good time-consuming process.

IV. CONCLUSION

Based on this study of whole system, the following limitations can be drawn:

In the world of simulations. D meteresigner need their designs to be quickly implemented on the lab for testing purposes. In Electronic industry simulation and practical implementation, both are necessary. Special emphasis on practical implementation is given, because electronics can behave differently when are assembled. For the lack of field programmable boards for Analog world is not acceptable. Our project is partially fulfilling that requirement. With development of programming software, this thing can come out loud in future!

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