International Journal of Scientific Research in Computer Science, Engineering and Information Technology
ISSN : 2456-3307 (www.ijsrcseit.com)
doi : https://doi.org/10.32628/IJSRCSEIT

Design and Performance Analysis of Over Current Relay under different Faults Scenarios

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Article Info
Volume 8, Issue 3
Page Number : 274-281

Publication Issue :
May-June-2022

Article History
Accepted: 01 June 2022
Published: 07 June 2022

ABSTRACT

This research work will develops an automatic tripping mechanism for the three-phase supply system, following a fault in the transmission line. Whenever there is a fault, this proposed system will sense the fault and restricts the flow of supply to the grid-substations which are compressed of control gears without occurring more damage to them. For handling faults with long and short duration 555 timers are implemented. For the mechanism of tripping activation some switches are utilized to inject fault artificially. In the event of a temporary fault, the circuit will automatically reset after a brief interruption, whereas in the event of a permanent fault, the circuit will remain tripped. This primarily considers four cases: LLLG temporary fault, LLLG permanent fault, LLL temporary fault, and LLL permanent fault. The main benefit of the project is that it saves the appliance, which prevents damage to the load. The system only knows if there is a fault or not, and if the fault is temporary, the supply is restored. If the fault is permanent, a permanent trip signal is sent to the relay, and the supply to the load is restricted.

Keywords : Overcurrent Relay, Grid, LLLG fault, LLL fault, 555 Times, Circuit Breaker

I. INTRODUCTION

A fault in a power system is any abnormality in the electric current flowing through it. The following is an example of a fault occurrence. The open circuit fault occurs when the current is messed up due to the fault and the occurrence of short circuit due to current bypassing with normal load. In a three-phase system, the fault may occur between one or more phases and ground, or only between the system's phases. In general, protective devices are used in transmission systems to detect fault conditions and cause circuit breakers or isolators to operate, thereby limiting the damage caused by the failure. A fault in a three-phase or poly-phase system may affect some phases (resulting in asymmetrical operation). If all the

phases are affected equally, it results in a symmetrical fault. Asymmetrical faults are more difficult to understand than symmetrical faults. To protect the power system transmission lines, faults must be accurately detected and isolated [1–2]. The control panel of a power system contains numerous alarms that detect signals from various protection techniques for various types of fault. These flaws are either balanced or unbalanced. Electric power utility engineers have long been fascinated by the subject of fault location. Many electrical faults result in mechanical damage, which must be repaired before the line can be reconnected. If the location of the fault is known or can be estimated with reasonable accuracy, the restoration process can be sped up. The ability to detect, isolate, locate, and repair these faults quickly is critical for ensuring a reliable power system operation. The authors' goals in [3] are to clearly define each fault-locating algorithm's input data criteria, quantify the various sources of fault-locating error, demonstrate the application of each algorithm in locating real-world transmission line faults, and provide recommendations for selecting the best fault-locating approach. However, it only applies to distribution networks. The authors of [4] investigate the effect of different fault-locating error sources on a small number of algorithms [5] are excellent references for impedance-based fault location algorithms. Unfortunately, the discussion is limited to one-ended methods, and [6] does not cover all of the IEEE C37.114 impedance-based fault location algorithms. Some of the researchers proposed other methods for based on impedance measurements, phasor measurements, neural networks, and traveling waves. This methods use single terminal data and the others use double terminal data. The location of the fault point is simply estimated utilizing voltage and current measurements taken at line ends. Fault location can be estimated with varying degrees of accuracy using appropriate mathematical models and algorithms. In single terminal methods, an extra assumption must be added to the model. This assumption reduces the accuracy of these methods. Some parameters such as source impedance, pre-fault data, and sampling frequency have a major effect on different algorithms [8]-[9]. As proposed in [10] a novel approach, in which new type of magnetic sensors are deployed at the tower location, and the magnetic field signals are acquired and sent back to monitoring center. Then the fault location can be found and the type of faults can be identified by analyzing the measured signals. This approach is advantageous over traditional approaches in that it is independent of the distributed line parameters and has a location error smaller than one span. The fast progress in magneto-resistance sensor technology can actually enable a lot of applications in transmission line monitoring applications [11]. As proposed in [12], [13] have proposed new accurate fault location method based on computing the voltage profiles along the line using two-end of the line. As we know, it is impossible to calculate the voltage profile using one terminal data for a faulted line. If we regard the faulted line as healthy line, we can get a voltage profile using single-ended data, although the profile is not true behind the fault point, we call this profile as “fictitious voltage profile”. As proposed in [14]-[15], some switches are implemented for injecting the faults. This paper proposes a novel terminology of reclosing mechanism in the supply line. Section-I describes about the introduction and literature of the existing methods, Section-II depicts about description of the system and Section-III explains about the protective proposed system, Section-IV explains about both experimental setup and simulation based results and the last section will depicts about the conclusion of this project compared to the conventional methods.

II. DESCRIPTION OF THE SYSTEM

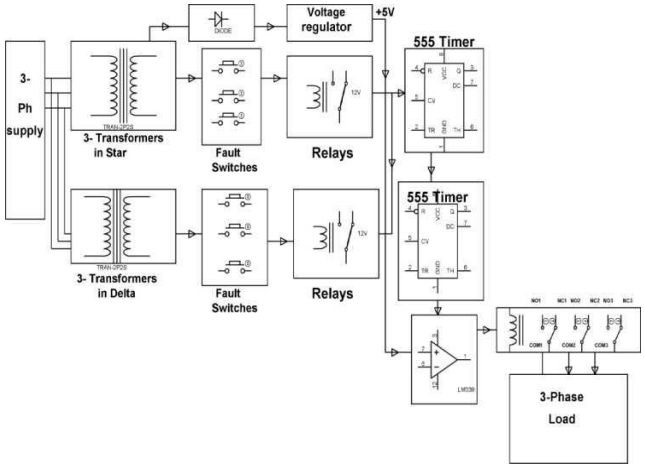


Figure 1: Experimental setup of the proposed system

The prototype model of the fault clearing system is shown in Figure 1. Six transformers known as step down transformers are primarily considered in this work for the analysis of faults in a three-phase system. The primary of three transformers is connected to a three-phase supply in a star configuration, and the secondary is also connected in a star configuration. The other set of three transformers has a three-phase primary connected in star and a delta secondary. Each of the six transformers' output is rectified and filtered separately before being routed to six relay coils. The six push buttons, one of which is connected across the relay coil, are designed to cause a fault condition at the star, such as LL Fault or 3 L Fault. All NC contacts on the relays are made parallel, and all common points are grounded. The parallel connected point of NC is fed to pin 2 of a 555 timer via a mono-stable resistor R5. Two 555ICs are used in the control circuit diagram of the fault clearing prototype, one in mono-stable mode and the other in isolated mode. The same timer's output is connected to the reset pin 4 of another mono-stable 5 5 5timer. LEDs are connected at their output to indicate their status. The U2 555 timer output from pin3 is connected to an Op-amp LM358 via wire 11 and dl2 to the non-inverting input pin3, while a potential divider RV2 keeps the inverting input at a constant voltage. The potential divider voltage at pin2 is held higher than the voltage at pin3 of the Op-amp used as a comparator, causing pinl to develop zero logic and fail to operate the relay via the driver transistor QI. This QI relay is a three-contact (3CO) relay, which means it is designed to disconnect the load in the event of a fault.

III. PROPOSED PROTECTIVE SYSTEM

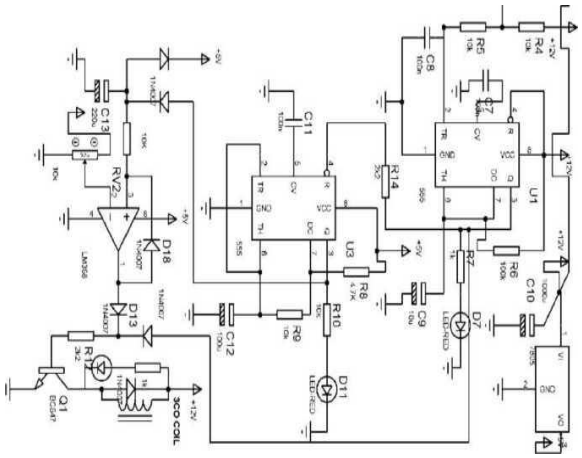


Figure 2 : Circuit Diagram of the proposed protective system

Whereas the panel is generated by a three-phase supply, all six relay coils receive DC voltage, and their common point disconnects from the NC and moves on to the NO points, providing logic high at pin2 of the mono-stable 555 timer U1. When any push button across the relay is pressed, it disconnects the relay and moves the common contacts to the NC position to provide a logic low at the 555 timer's trigger pin to develop an output that brings the U3 555 timer, which is used in a stable mode for its reset pin, to high such that the mono-stable operation takes place at its output, which is also indicated by flashing LED of D1.

If the fault is transitory, i.e. if the switch is activated and quickly released, the U1 mono-stable disables U3, causing its output to be zero. If the push button is held down for an extended period of time, the mono-stable output provides a longer duration active situation for U3, the astable timer, the output of

which charges capacitor Cl 3 through R11, causing the comparator output to go high and the relay to turn off. Because of positive feedback provided by a forward reverse biased and a series resistor, the Op-output amp's remains high indefinitely. As a result, the relay remains activated indefinitely to disconnect the load connected at its NC contacts. To keep the DC supply flowing, the star-connected secondary set DC's are paralleled through D8, D9, and D10 to provide an uninterrupted supply to the 12v DC and 5v DC circuit voltages derived from voltage regulator IC 7805.

IV. RESULTS AND DISCUSSION

The analysis of faults has been done through the simulation based results. The simulation results are evaluated by using Matlab/Simulink Software. Mainly two types of faults are considered namely Line-line-line-ground (LLLG) fault and line-line-line (LLL) fault. This fault types are majorily focused on current and voltage components. The occurrence of faults will be of cases permanent fault and temporary fault.

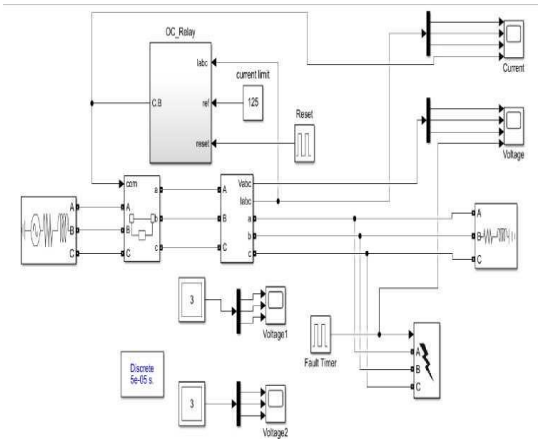


Figure 4 : Simulation diagram for fault analysis

The above figure-4 will depicts about the simulink model of the proposed system. In this the supply is taken from the 3-phase AC supply and a circuit breaker is connected make or break the circuit at the time of fault occurrence. An overcurrent relay is connected to the circuit breaker. A switch is connected for the creation of fault in the system. The obtained output is given to the load. Fault is injected in between the supply and load. The faults considered in this work, are of two types LLLG fault and LLL fault in two modes permanent mode and temporary mode with voltage and current components.

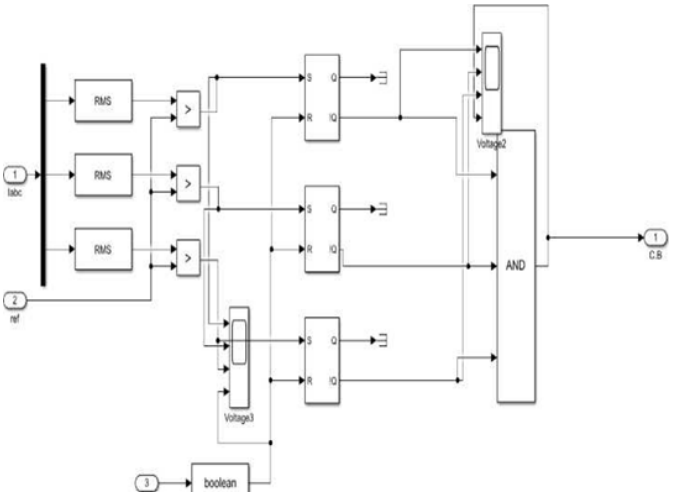
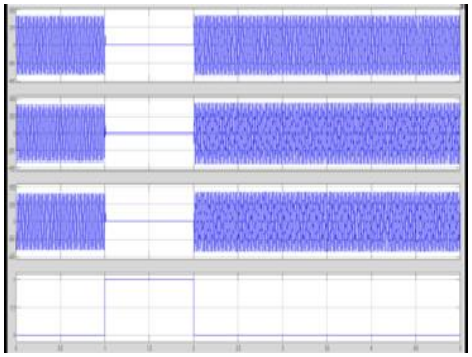


Figure 5: Simulink Model of Overcurrent Relay

The relay which is operating when the current exceeds the preset value is known as overcurrent relay. The simulink model of overcurrent relay is depicted in the above figure-5. In this work the instantaneous overcurrent is implemented. If the RMS currents is greater than the reference current then the circuit breaker will goes to trip position. So by this we can conclude that the fault has been occurred in the system. This related results of simulation are depicted below.

A. Case-i: LLLG Temporary Fault:

In this case line-line-line-ground fault in temporary mode is considered and the obtained voltage and current related results are shown below. Momentary disruptions are caused by temporary faults.



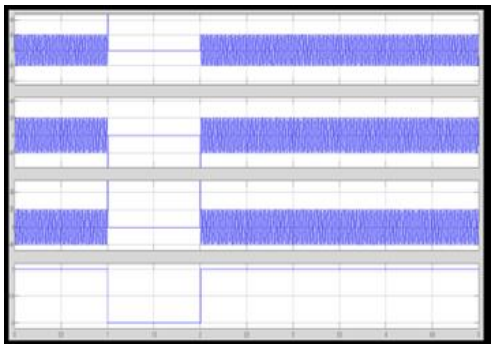
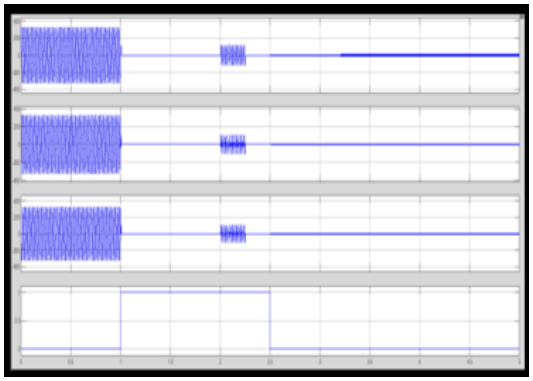


Figure 6: Simulation based results of LLLG temporary faults occurred in Voltage and Current

From the above figures it can be depicted that the waveform of voltage is in sinusoidal constant from 0s to 1s with amplitude of 320V and from 1s to 2s the amplitude is decreased to 0 due to occurrence of fault and goes to normal position once after the fault is cleared. In the similar manner the waveform of the current is in sinusoidal form with a value ranging from -20V to 20V and it is decreased to 0V due to occurrence of fault and it comes to normal position once after the fault is cleared. This is the temporary LLLG fault.

Case-ii: LLLG Permanent Fault:

Permanent faults causes sustained disruption if not cleared by protection. In this case Line-line-line-ground fault is in permanent mode. The obtained current and voltage waveforms are depicted below.



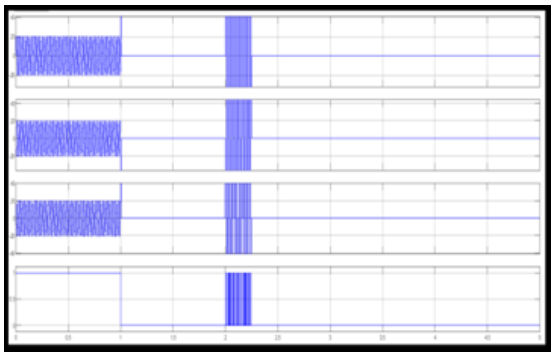
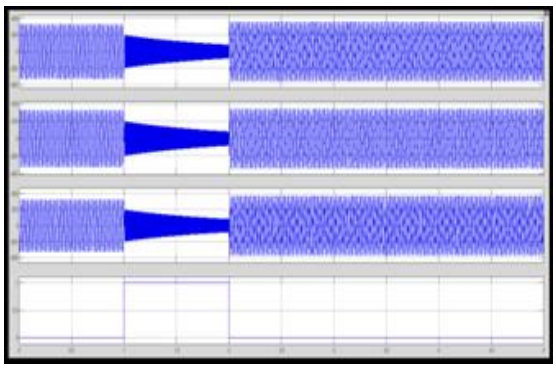


Figure 7 : Simulation based results of LLLG permanent faults occurred in Voltage and Current

In this case-ii, the waveform of the voltage is in sinusoidal from 0s to 1s with a value ranging from -320V to 320V, at 2s the amplitude of the waveform is decreased to zero and it continues the same till 5s with some distortions due to unavailability of protecting circuit or device. In the similar manner the waveform of the current is in sinusoidal form with a value ranging from -20V to 20V and it is decreased to 0V due to occurrence of fault and it still continues upto 5s due to unavailability of protecting device. This is permanent LLLG fault.

Case-iii: LLL Temporary Fault:

Case-iii: LLL Temporary Fault:



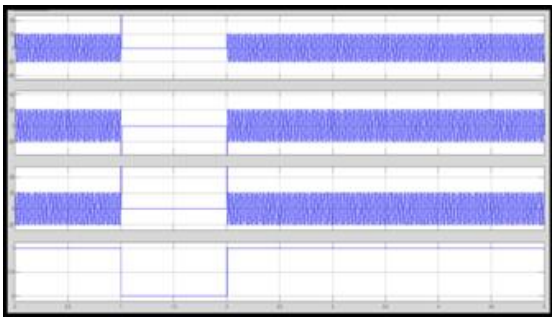
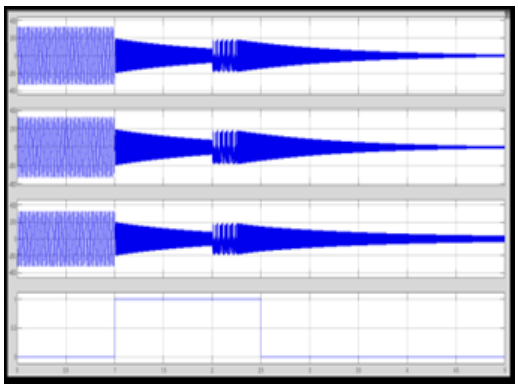


Figure 8: Simulation based results of LLL temporary faults occurred in voltage and current

From the above figures it can be depicted that the waveform of voltage is in sinusoidal constant from 0s to 1s with amplitude of 320V and from 1s to 2s the amplitude is decreased to -200V to 200V due to occurrence of fault and goes to normal position once after the fault is cleared. In the similar manner the waveform of the current is in sinusoidal form with a value ranging from -20V to 20V and it is decreased to 0V due to occurrence of fault and it comes to normal position once after the fault is cleared. This is the temporary LLLG fault occurred in voltage and currents.

Case-iv: LLL Permanent Fault



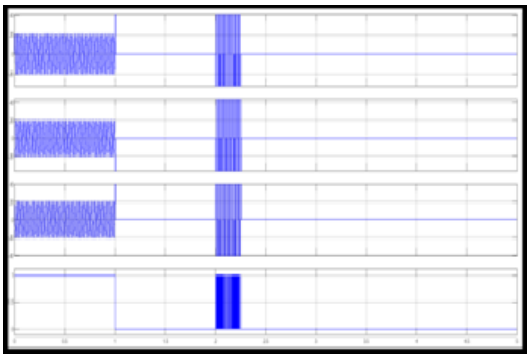


Figure 9: Simulation based results of LLL permanent faults occurred in Voltage and Current

In this case-ii, the waveform of the voltage is in sinusoidal from 0s to 1s with a value ranging from -320V to 320V, at 2s the amplitude of the waveform is decreased and varies from -200V to 200V and it continues the same till 5s with some distortions due to unavailability of protecting circuit or device. In the similar manner the waveform of the current is in sinusoidal form with a value ranging from -20V to 20V and it is decreased to 0V due to occurrence of fault and it still continues upto 5s due to unavailability of protecting device. This is permanent LLL fault.

V. CONCLUSION

In this research work, design and performance analysis of overcurrent relay under different scenarios is implemented. Whenever there is a fault, this proposed system will sense the fault and restricts the flow of supply to the grid-substations which are compressed of control gears without occurring more damage to them. For handling faults with long and short duration 555 timers are implemented. For the mechanism of tripping activation some switches are utilized to inject fault artificially. Mainly four cases are considered namely LLLG temporary fault, LLLG permanent fault and LLL temporary fault, LLL permanent fault. These faults are evaluated in voltage and current waveforms. For analyzing the faults 555 timer has been used with relay. The simulation results

of this proposed system is implemented by using Matlab/Simulink Software.

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Cite this article as :

O. Thireesh, N. Sudarsan Rao, D. Jeevan Kumar Reddy, D.Amulya, CH. Malavika, K. V. Dileep Kumar, "Design and Performance Analysis of Over Current Relay under different Faults Scenarios ", International Journal of Scientific Research in Computer Science, Engineering and Information Technology (IJSRCSEIT), ISSN : 2456-3307, Volume 8 Issue 3, pp. 274-281, May-June 2022.
Journal URL : https://ijsrcseit.com/CSEIT228384