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Use Of MGDI Technique to Implement Low Power and Region Efficient 4 Bit ALU

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ABSTRACT

When compared to GDI technology, the improved GDI technology is significantly more efficient in terms of power utilisation, power complexity, and low voltage output. A 4-bit arithmetic logic unit (ALU) was built using a revised gate diffusion input technique and a compact all-transistor adder with a modest transistor footprint and throughput in this project. It has a high rate of reusability and is cost-effective. When compared to traditional CMOS technology, low power consumption is nearly equal. The 4-bit Arithmetic Logic Unit (ALU) is a structure created by the Micro wind tool in the DSCH 3.5 MGDI format. The simulation was run using 65nm technology with a 1.2V voltage. GDI and GDI modifications were used to design the 4-bit ALU and its blocks. In comparison to previous efforts, the results show that the proposed architecture reduces power consumption by lowering the number of transistors while achieving entirely adaptive performance.

Index Terms - ALU, gate spread input (GDI), modified GDI, low power

I. INTRODUCTION

Low power, swift speed, and tiny plan area switching are three points that the market expressly wants. As a result, research into low-power, high-speed embedded systems for cell phones and laptop has progressed to the point where dynamic operation on a single chip is now viable. Because power and space are important considerations when employing an ALU, we recommend low power or GDI's rational design style. When compared to other designs now in use, such as CMOS, PTL, CPL, and TG, this technique can reduce the number of transistors to reduce power consumption and propagation delay. GDI technology is used in the ALU and its blocks. The complexity of production and energy usage are, however, negligible when using decommissioned GDI technology. As a result, a modified GDI has been proposed. In comparison to GDI

technology, Modified Gate Diffuse Input (MODGDI) technology provides the best performance in terms of power utilisation, power complexity, and low result voltage.

An Adder is a place where the ALU is built. The ALU was designed using a multiplexer and a complete Adder circuit, as recommended by Arkadiy Morgenshtein, Idan Schwartz, and Alexander Fish [1]. This cycle considers the execution of a grouping of mind-boggling logical tasks employing the primary two semiconductors, as shown in Table I. As shown in Figure 1, the initial GDI was based on the use of a basic cell.

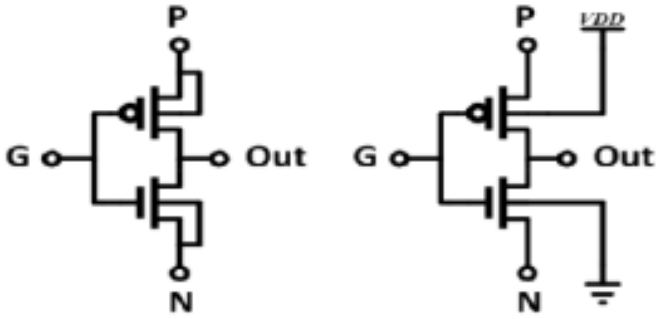

Fig.1 (i) Basic GDI cell (ii) Standard CMOS compatible

However, compared to CMOS and PTL technologies, manufacture on twin-well MOS or silicon-on-insulator (SOI) method has been proposed, which can improve the power consumption, delay, and area of digital circuits. The disadvantage of GDI cells was that they had lower voltage amplitude due to lower thresholds, which resulted in worse performance and more static power loss. Morgenstern [2] Figure 1 shows a modified GDI technique that was suggested (ii). GND and VDD are always assigned individually to the board terminals of NMOS and MIMO semiconductors in this approach. As a result of this improvement, GDI cells may now be fabricated using regular CMOS methods. In comparison to the twin well and (SOI) methods, this is less expensive.

TABLE I LOGIC FUNCTIONS REALIZATION USING GDI CELL

N	P	G	OUTPUT	FUNCTION
0	1	A	A’	INVERTER
0	B	A	A’B	F1
B	1	A	A’+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MUX
B’	B	A	A’B+B’A	XOR
B	B’	A	AB+A’B’	XNOR

The plan for a 4-bit arithmetic logic unit (ALU) employing the modified gate diffuse input method is presented in this paper provides a complete adder block and compares the outcome to the previous work. DSCH tools and Micro wind software are used to analyse performance. Micro wind combines front and back configurations into a single coordinated flow, decreasing design complexity and speeding up the design process. It oversees highly integrated signal processing and digital implementation, as well as circuit simulation, semiconductor-level

output, and verification. Using 6 metal layer CMOS technology, DSCH, and Micro wind software tools, performance boundaries such as ALU location, power consumption, and propagation delay are investigated at 65 nm.

II. ARITHMETIC LOGIC UNIT

In this project, we will use the MGDI method to identify the circuit. The components required for ALU design are:

A. 2x1 Multiplexer

A multiplexer is a computerized switch that chooses the result of numerous data sources in view of the chose signal [4], as displayed in Figure 2. A 2x1 multiplexer with two semiconductors.

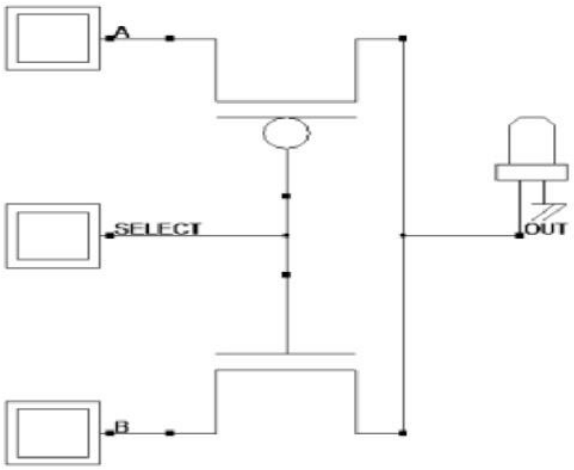

Fig 2. MGDI Based 2x1 Multiplexer

B. 4x1 Multiplexer

As demonstrated in Figure 3, the 2x1 multiplexer above produces a 4x1 multiplexer with only six transistors.

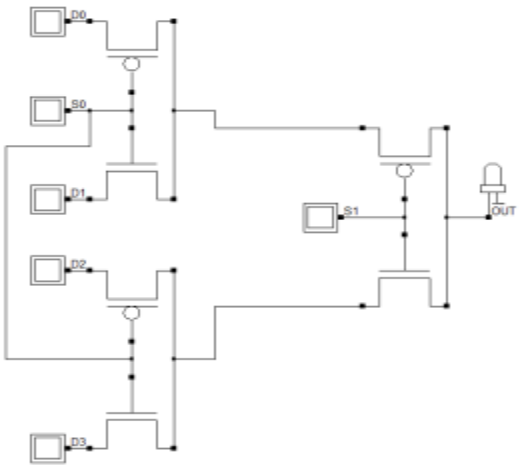

Fig 3 MGDI GDI 4x1 Multiplexer

C. Full Adder

A complete adder is a series-parallel circuit that adds three input bits to produce an arithmetic sum. It has three inputs and two effects. To detect AND, OR, and XOR, the adder cell in this design uses a full swing gate. With certain tweaks, this architecture offers low power consumption, very low latency, and performs logical functions such as OR, AND, XOR, and XNOR. The majority of the ALU plan is saved using these progressions.

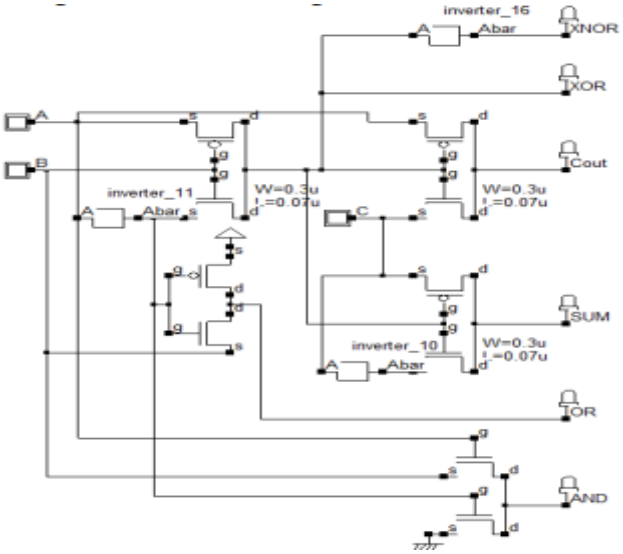

Fig 4 Full Adder cell for ALU

III. DESIGN OF ALU

The ALU is a significant part of the central processing unit (CPU) of every PC and is also included in the base chip. It is responsible for handling numbers. B. Expansion, deduction, duplication, reduction, and consistent capacity. B. AND, OR, XOR and XNOR [6].

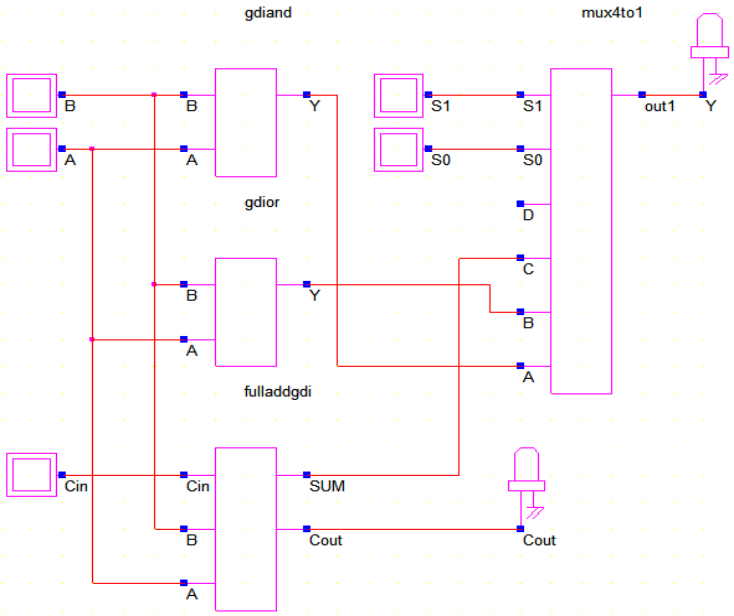

Fig 5 GDI-based 1-bit ALU phase schematic Design

The 4-bit ALU design employing GDI logic is shown in figure (8). The 4-bit ALU consists of three selection bits, eight 411 MUX, eight 211 MUX, and four processing units.

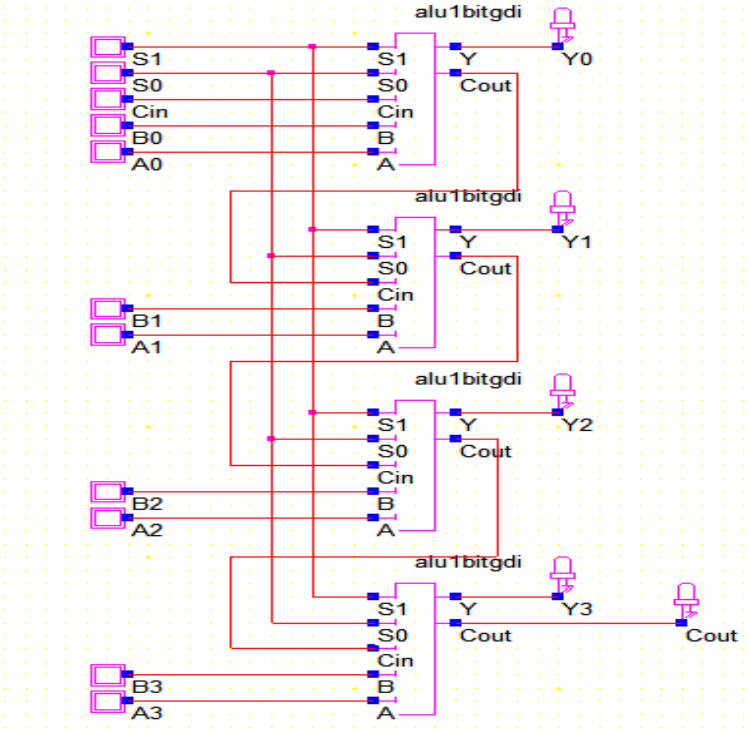

Fig 6 Schematic of 4-Bit ALU Stage using GDI

The proposed design for a 4-bit arithmetic logic unit consists of four stages, each of which is a 1-bit ALU block, and the circuit is as follows: For a complete swing cell design, two 2x1 multiplexers, two 4x1 multiplexers, and 48 semiconductors are required for each 1-bit ALU stage, as shown in Figure 5. On the destination lines S0, S1, and S2, you can do any desired activity on the code. The suggested ALU reality tables are summarised in Table II. To execute decrement, expansion, and To, the 4x1 multiplexer for information determines the B input for the top of the destination lines S0 and S1 to choose from Reason 1, B, B', and Reason 0 to do decrement, expansion, and To. S2 chooses a numerical or reasoning exercise after completing the subtraction and increment assignments independently.

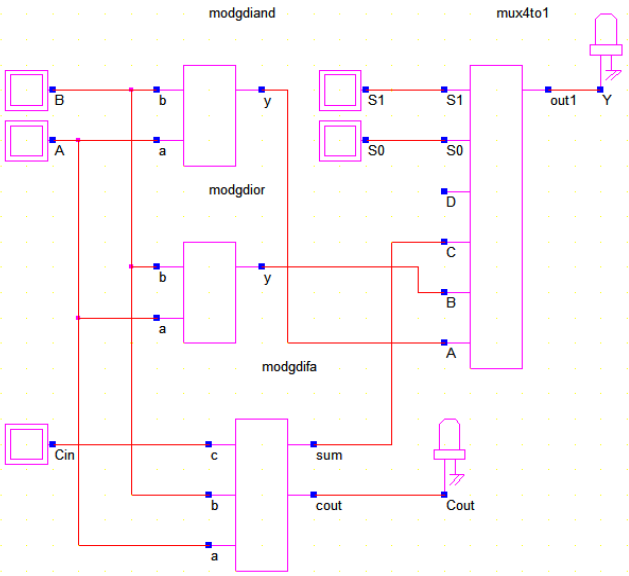

Fig 7 Schematic of 1-Bit ALU Stage using MGDI

Figure 6 shows the four processes utilised to create a 4-bit ALU. The carry input of ALU0, on the other hand, is connected to the selection line S1 and receives the logical 1 required for the subtract and increment operations, while the other values have no effect on the logical operation's outcome.

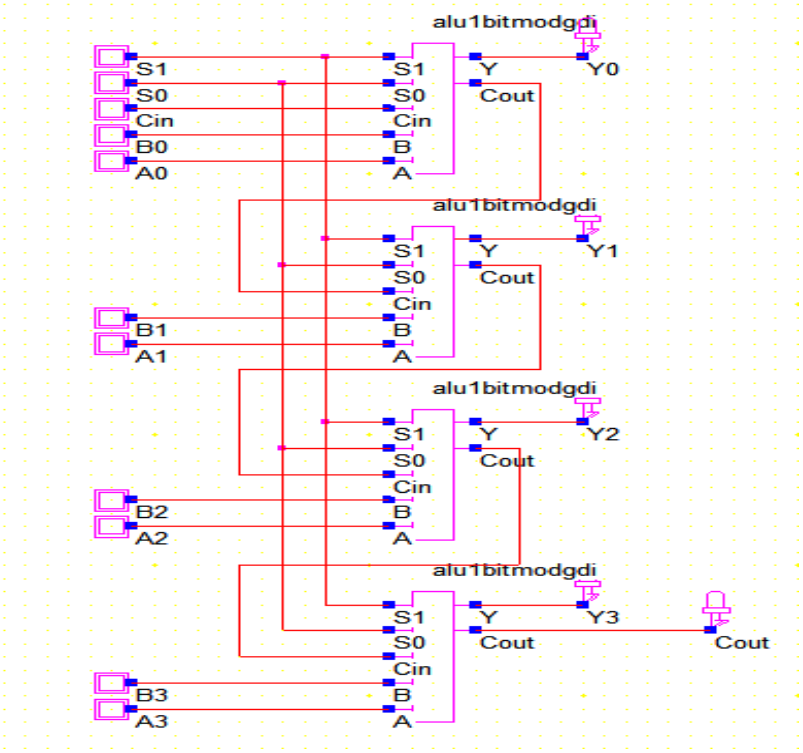

Fig 8 Schematic of 4-Bit ALU Stage using MGDI

IV. SIMULATION RESULTS

A. GDI Technique

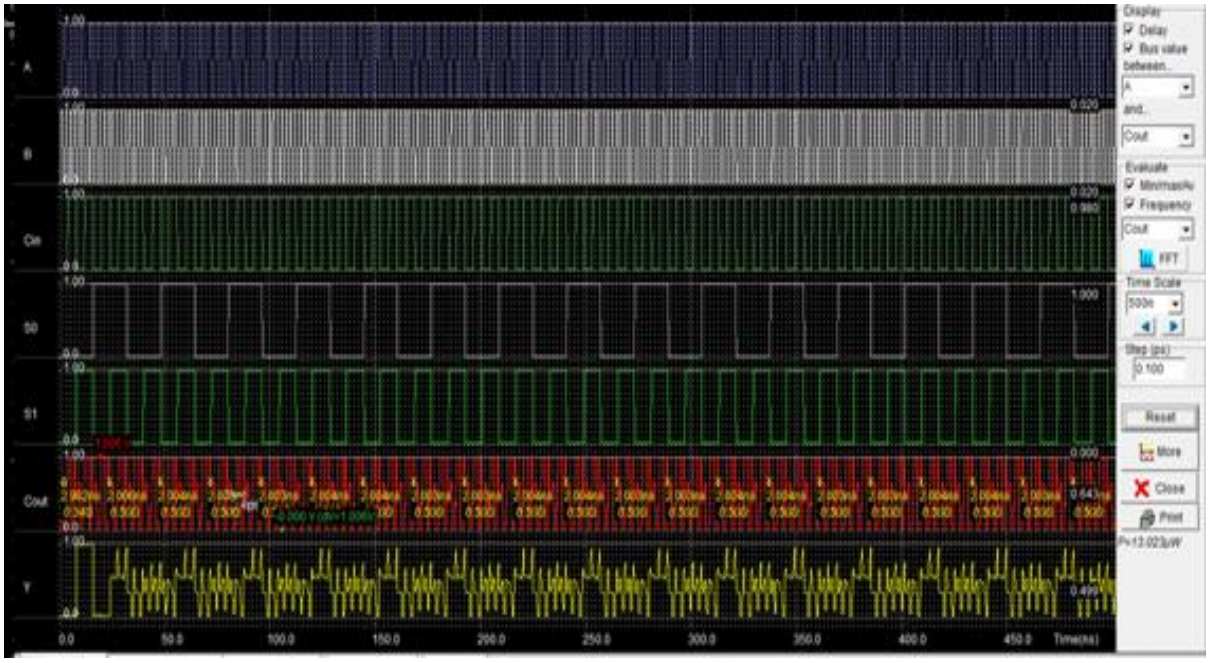

Fig 9 Simulation Output of 1-Bit ALU Stage using GDI

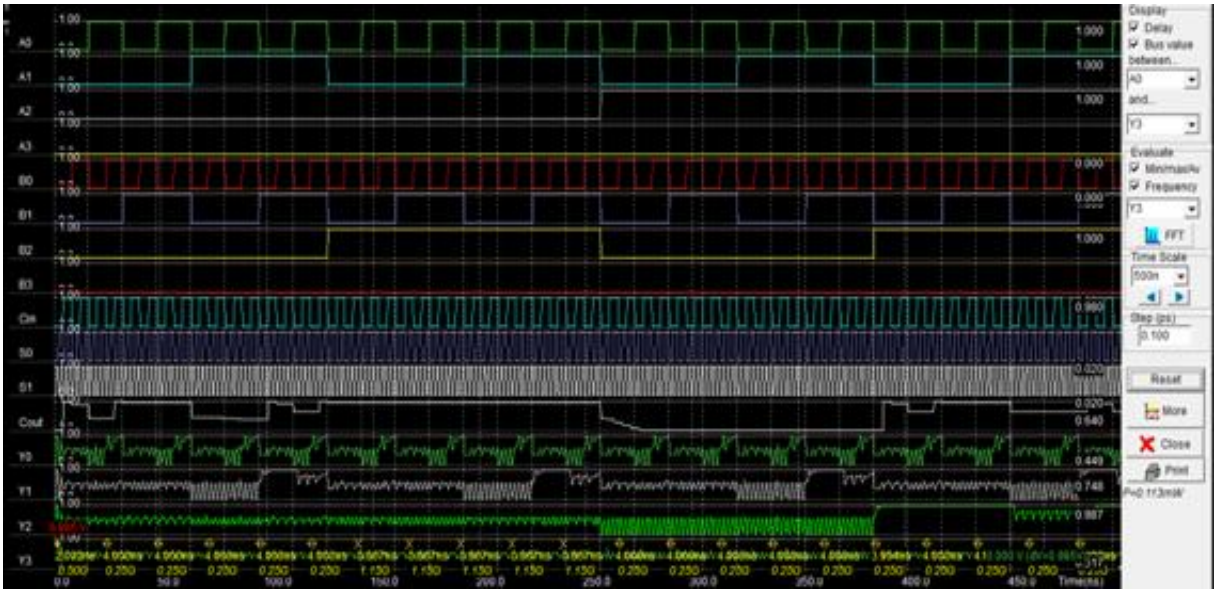

Fig 10 Simulation Output of 4-Bit ALU Stage using GDI

Using 65nm CMOS layout design principles, the existing 1-bit and 4-bit ALUs facing the GDI circuit were configured. The polymerase size (W: 0.5um, L: 0.07m) and MIMO size (W: 0.3m, L: 0.07m) both enhance performance and delay execution. A DSCH and Micro wind based test system with 1.2V power supply were used to complete the replica. The ALU waveform based on the GDI method is shown in Figures 9 and 10, with A, B, and C as test inputs and S2, S1, and S0 as selection information. The design outcomes of the GDI technology are shown in Tables II and III in comparison to the 1-bit ALU and 4-bit ALU designs.

B. Modified GDI Technique

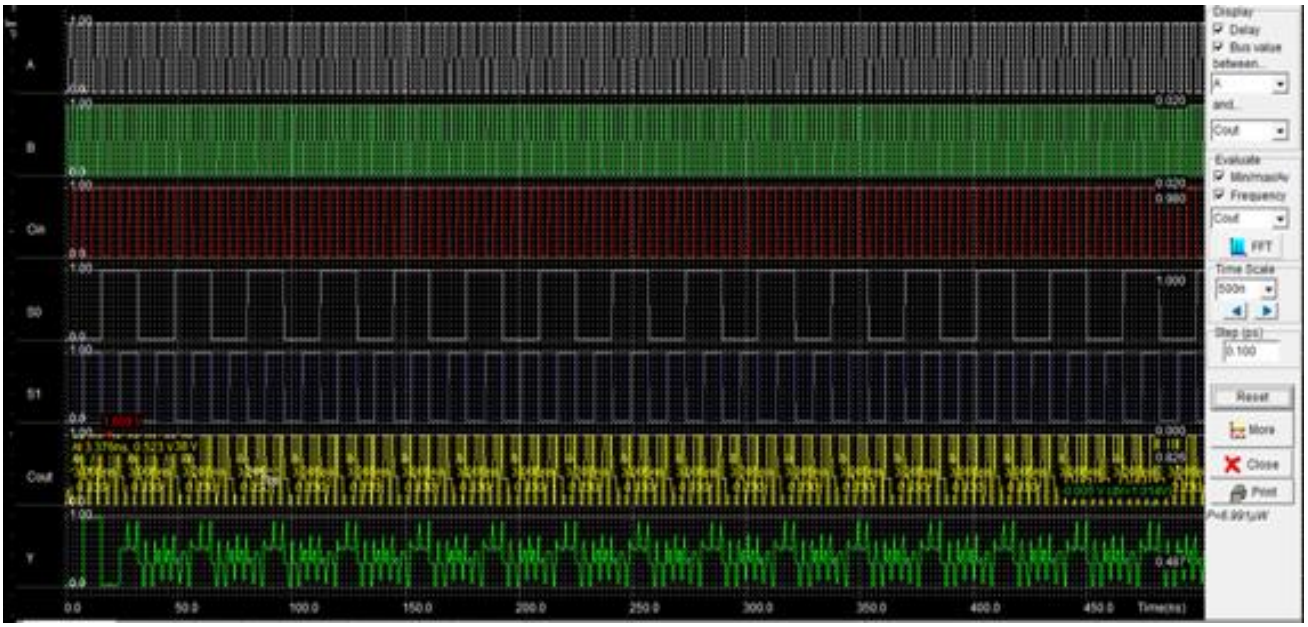

Fig 11 Simulation Output of 1-Bit ALU Stage using MGDI

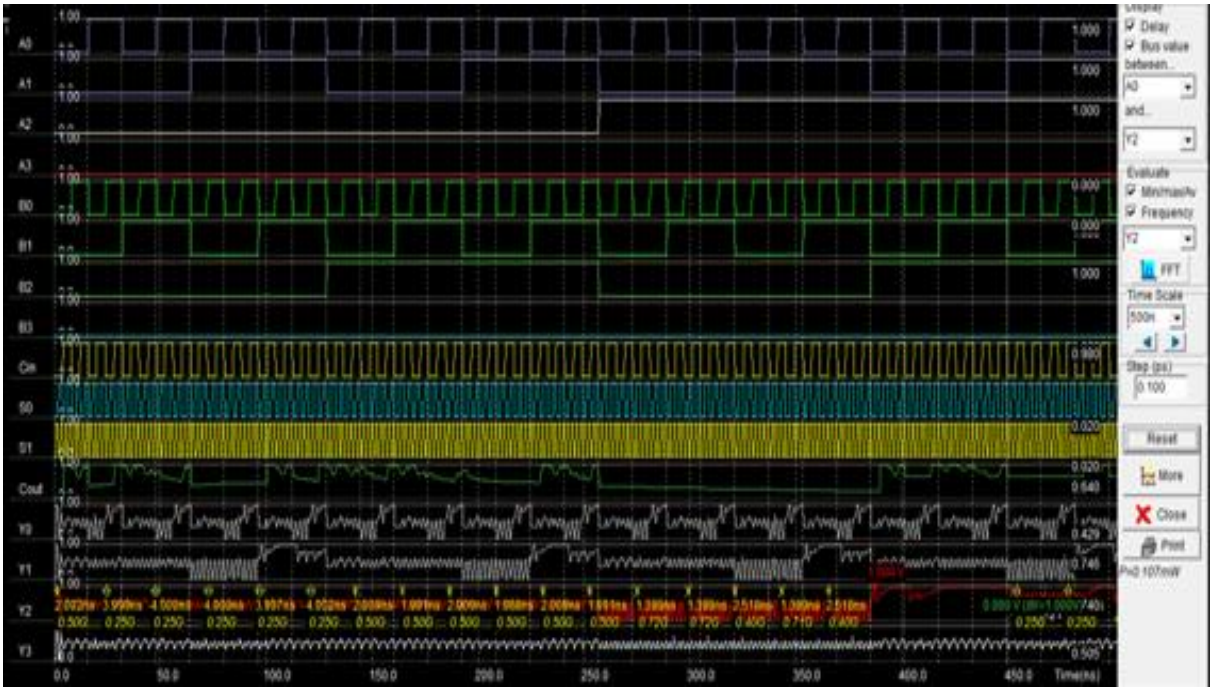

Fig 12 Simulation Output of 4-Bit ALU Stage using MGDI

Using 65nm CMOS layout design principles, the proposed 1-bit and 4-bit ALU circuits for the MGDI technology were arranged. The polymerase size (W: 0.5um, L: 0.07 m) and MIMO size (W: 0.3 m, L: 0.07 m) provide poor performance and cause execution delays. A DSCH and Micro wind based test system with 1.2V power supply were used to complete the replica. Figures 11 and 12 show the ALU waveforms for the MGDI method design in Tables II and III, with A, B, and C as test inputs and S2, S1, and S0 as selection information.

C. Comparison Results

TABLE II: COMPARISON OF 1-BIT ALU

Parameters	Number of transistors used	Area utilized	Power dissipation	Delay
CMOS based ALU	54	19.7%	34.832uW	1.998ns
GDI based ALU	20	13.4%	13.023uW	2.982ns
Modified GDI based ALU	18	12.4%	6.991uW	3.006ns

For a 1-bit ALU, the modified GDI-based ALU has 10% fewer transistors than the GDI-based ALU and 66.67% less than the CMOS-based ALU. The area used by the modified GDI-based ALU is less than 7.46% compared to the GDI-based ALU and 37.05% compared to the CMOS-based ALU. The modified GDI-based ALU consumes less than 46.318% compared to the GDI-based ALU and 79.92% compared to the CMOS-based ALU. But compromises or compromises are delayed. H. The delay is increased by 0.8% for the modified GDI-based ALU compared to the GDI-based ALU and 50.48% compared to the CMOS-based ALU.

TABLE III: COMPARISON OF 4-BIT ALU

Parameters	Number of transistors used	Area utilized	Power dissipation	Delay
CMOS based ALU	216	50.9%	0.1mW	8ns
GDI based ALU	80	45.6%	0.113mW	2.002ns
Modified GDI based ALU	72	45.7%	0.107mW	2.002ns

For a 4-bit ALU, the modified GDI-based ALU has less than 10% transistors compared to the GDI-based ALU and 66.67% compared to the CMOS-based ALU. The area used by the modified GDI-based ALU is 0.2% larger than the GDI-based ALU and 10.216% smaller than the CMOS-based ALU. The modified GDI-based ALU consumes less than 5.3% compared to the GDI-based ALU and 7% more than the CMOS-based ALU. The delay is reduced by 0% for the modified GDI-based ALU compared to the GDI-based ALU and 74.97% compared to the CMOS-based ALU.

V. CONCLUSION

This project shows how to plan a 4-bit ALU in a 65 nm CMOS layout using the MGDI method and model it using the DSCH and Micro wind templates. The re-enactment findings show that the proposed ALU design improves power utilisation and semi-conductor count while maintaining full-swing function. The proposed architecture uses 72 semiconductors and runs on a 1.2V supply voltage.

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